

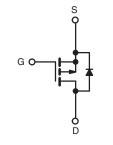


Power MOSFET

PRODUCT SUMMA	RY			
V _{DS} (V)	-100			
R _{DS(on)} (Ω)	V _{GS} = -10 V	1.2		
Q _g (Max.) (nC)	8.7			
Q _{gs} (nC)	2.2			
Q _{gd} (nC)	4.1			
Configuration	Single			



Marking code: FF



P-Channel MOSFET

FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- · Repetitive avalanche rated
- P-channel
- · Fast switching
- Ease of paralleling
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mount using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION		
Package	SOT-223	SOT-223
Lead (Pb)-free and Halogen-free	SiHFL9110-GE3	SiHFL9110TR-GE3 ^a
Lood (Dh) free	IRFL9110PbF	IRFL9110TRPbF ^a
Lead (Pb)-free	SiHFL9110-E3	SiHFL9110T-E3 ª

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	-100	V	
Gate-Source Voltage		V _{GS}	± 20	v	
Continuous Drain Current	V = 10.V	T _C = 25 °C		-1.1	
Continuous Drain Current V_{GS} at - 10 V $\frac{1}{T_{GS}}$		T _C = 100 °C	ID	-0.69	А
Pulsed Drain Current ^a		I _{DM}	-8.8		
Linear Derating Factor			0.025	W/°C	
Linear Derating Factor (PCB Mount) ^e			0.017	W/ C	
Single Pulse Avalanche Energy ^b			E _{AS}	100	mJ
Avalanche Current ^a		I _{AR}	-1.1	А	
Repetitive Avalanche Energy ^a		E _{AR}	0.31	mJ	
aximum Power Dissipation $T_{\rm C} = 25 ^{\circ}{\rm C}$		D	3.1	w	
Maximum Power Dissipation (PCB Mount) ^e	T _A =	25 °C	PD	2.0	vv
Peak Diode Recovery dV/dt ^c		dV/dt	-5.5	V/ns	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C	
Soldering Recommendations (Peak Temperature) ^d	for	10 s		300	U

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = -25 V, starting T_J = 25 °C, L = 7.7 mH, R_g = 25 Ω , I_{AS} = -4.4 A (see fig. 12).

c. $I_{SD} \leq -4.4$ A, dl/dt ≤ -75 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

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FREE



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R _{thJA}	-	-	60	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		-		•	•		
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	= 0 V, I _D = -250 μA	-100	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = -1 mA	-	-0.091	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = -250 μA	-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}		$V_{GS} = \pm 20 V$		-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}		-100 V, V _{GS} = 0 V 7, V _{GS} = 0 V, T _J = 125 °C	-	-	-100 - 500	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -0.66 A ^b	-	-	1.2	Ω
Forward Transconductance	9 _{fs}	V _{DS} =	-50 V, I _D = -0.66 A	0.82	-	-	S
Dynamic							
Input Capacitance	C _{iss}		$V_{GS} = 0 V$,	-	200	-	
Output Capacitance	C _{oss}		$V_{\rm GS} = -25 \rm V,$		94	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1	.0 MHz, see fig. 5	-	18	-	
Total Gate Charge	Qg			-	-	8.7	
Gate-Source Charge	Q _{gs}	$V_{GS} = -10 V$	I _D = -4.0 A, V _{DS} = -80 V, see fig. 6 and 13 ^b	-	-	2.2	nC
Gate-Drain Charge	Q _{gd}			-	-	4.1	
Turn-On Delay Time	t _{d(on)}			-	10	-	
Rise Time	t _r	V _{DD} =	-50 V, I _D = -4.0 A,	-	27	-	
Turn-Off Delay Time	t _{d(off)}	$R_{G} = 24 \Omega,$	$R_D = 11 \Omega$, see fig. 10 ^b	-	15	-	ns
Fall Time	t _f	- 17		-			
Internal Drain Inductance	L _D	Between lead 6 mm (0.25")	, <u> </u>	-	4.0	-	- nH
Internal Source Inductance	L _S	package and die contact	center of	-	6.0	-	
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET sym showing the	MOSFET symbol		-	-1.1	A
Pulsed Diode Forward Current ^a	I _{SM}	integral revers p - n junction		-	-	-8.8	
Body Diode Voltage	V_{SD}	T _J = 25 °C	$I_{\rm S}$ = -1.1 A, $V_{\rm GS}$ = 0 V ^b	-	-	-5.5	V
Body Diode Reverse Recovery Time	t _{rr}	T 05 °O J	- 40 A dl/dt 100 A/ b	-	80	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$J = 25 C, I_F$	= -4.0 A, dl/dt = 100 A/µs ^b	-	0.15	0.30	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn	-on is dor	ninated b	v Ls and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width \leq 300 µs; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

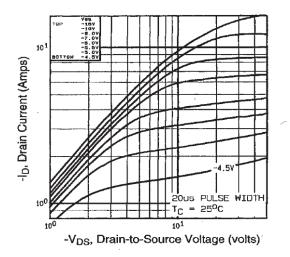


Fig. 1 - Typical Output Characteristics

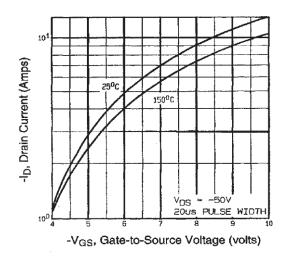


Fig. 3 - Typical Transfer Characteristics

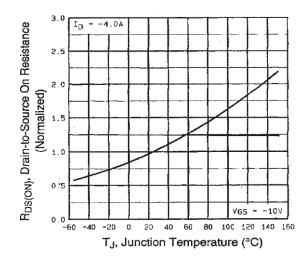


Fig. 4 - Normalized On-Resistance vs. Temperature

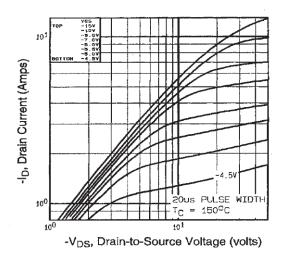


Fig. 2 - Typical Output Characteristics





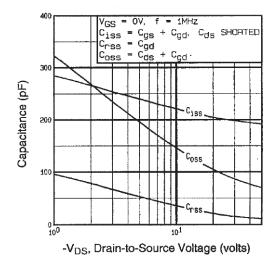


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

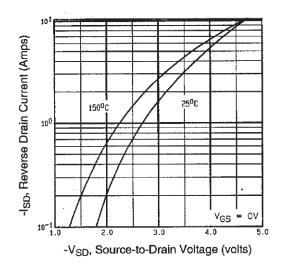


Fig. 7 - Typical Source-Drain Diode Forward Voltage

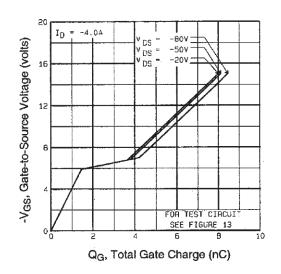


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

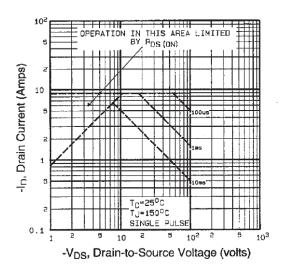


Fig. 8 - Maximum Safe Operating Area



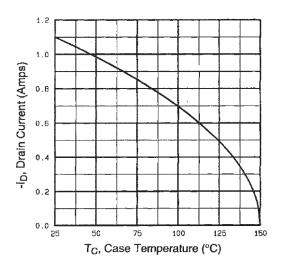


Fig. 9 - Maximum Drain Current vs. Case Temperature

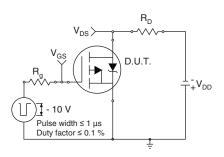


Fig. 10a - Switching Time Test Circuit

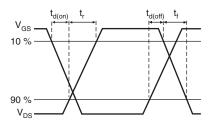


Fig. 10b - Switching Time Waveforms

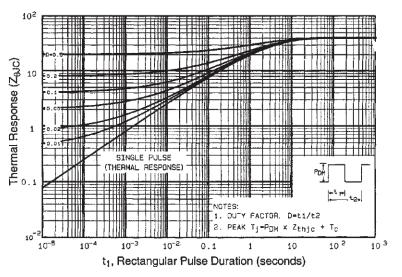


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



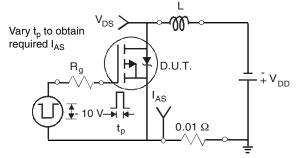
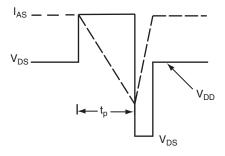


Fig. 12a - Unclamped Inductive Test Circuit



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Fig. 12b - Unclamped Inductive Waveforms

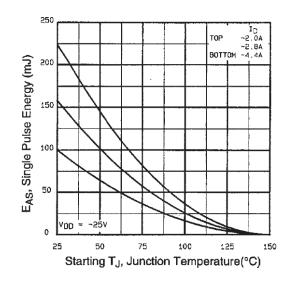


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

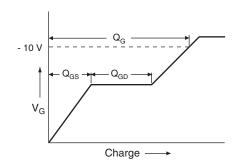


Fig. 13a - Basic Gate Charge Waveform

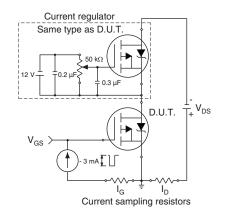


Fig. 13b - Gate Charge Test Circuit

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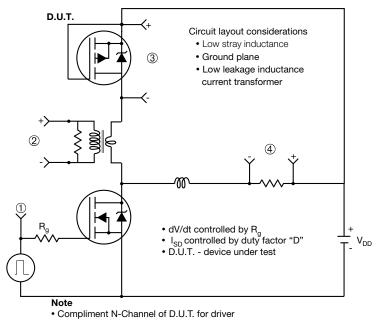
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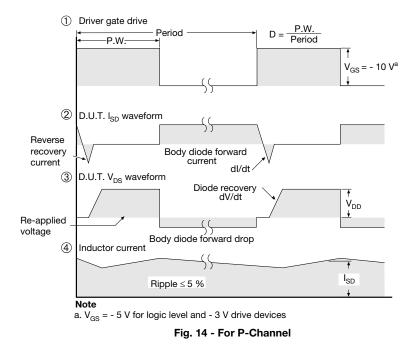
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Peak Diode Recovery dV/dt Test Circuit

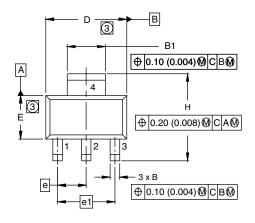


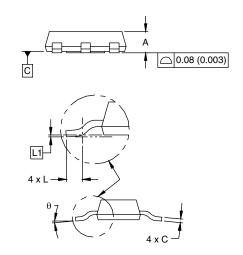


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SOT-223 (HIGH VOLTAGE)





	MILLI	METERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	1.55	1.80	0.061	0.071	
В	0.65	0.85	0.026	0.033	
B1	2.95	3.15	0.116	0.124	
С	0.25	0.35	0.010	0.014	
D	6.30	6.70	0.248	0.264	
E	3.30	3.70	0.130	0.146	
е	2.30	2.30 BSC		0.0905 BSC	
e1	4.60	BSC	0.181	BSC	
Н	6.71	7.29	0.264	0.287	
L	0.91	-	0.036	-	
L1	L1 0.061 BSC		0.002	4 BSC	
θ	-	10'	-	10'	

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Dimensions are shown in millimeters (inches).

3. Dimension do not include mold flash.

4. Outline conforms to JEDEC outline TO-261AA.



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