

bq296xxx Overvoltage Protection for 2-Series, 3-Series, and 4-Series Cell Li-Ion Batteries with Regulated Output Supply

1 Features

- 2-Series, 3-Series, and 4-Series Cell Overvoltage Protection (OVP)
- Fixed Delay Timer to Trigger FET Drive Output (3-s, 4-s, 5.5-s or 6.5-s Options)
- Factory Programmed OVP Threshold (Threshold Range 3.85 V to 4.6 V)
- Output Options: Active High
- High-Accuracy Overvoltage Protection: ± 10 mV
- Regulated Supply Output With Self-Disable and/or External Enable/Disable Control
 - Options: 3.3-V, 2.5-V, and 1.8-V (bq2960, bq2961)
 - Options: 3.3-V, 3.15-V, 3.0-V (bq2962)
- Low Power Consumption $I_{CC} \approx 4$ μ A ($V_{CELL(ALL)} < V_{PROTECT}$)
- Extra Low Power Consumption With REG Output Disabled, $I_{CC} \sim 1.2$ μ A
- Low Leakage Current Per Cell Input < 100 nA
- Small Package Footprint
 - 8-Pin WSON (2 mm \times 2 mm)

2 Applications

- Notebook PC
- Ultrabooks
- Medical
- UPS Battery Backup

3 Description

The bq296xxx family is a high accuracy, low power overvoltage protector with a 1-mA regulated output supply for Li-Ion battery pack applications.

Each cell in a 2-series to 4-series cell stack is individually monitored for an overvoltage condition. An internally fixed-delay timer is initiated upon detection of an overvoltage condition on any cell; upon expiration of the delay timer, an output pin is triggered into an active state to indicate that an overvoltage condition has occurred.

The regulated output supply delivers up to 1-mA (max) output current to drive always-on circuits, such as a real-time clock (RTC) oscillator. The bq296xxx family has a self-disable function to turn off the regulated output if any cell voltage falls below a certain threshold, thereby preventing drain on the battery, and provides an external control to enable or disable the regulated output.

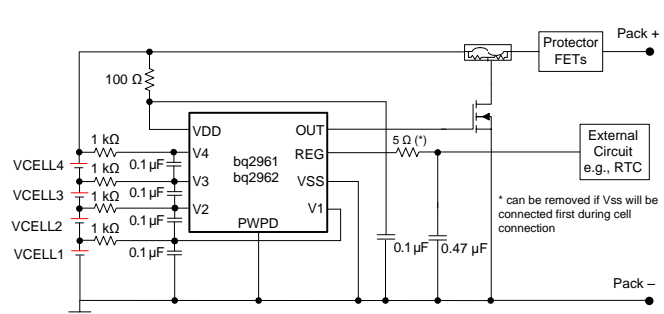
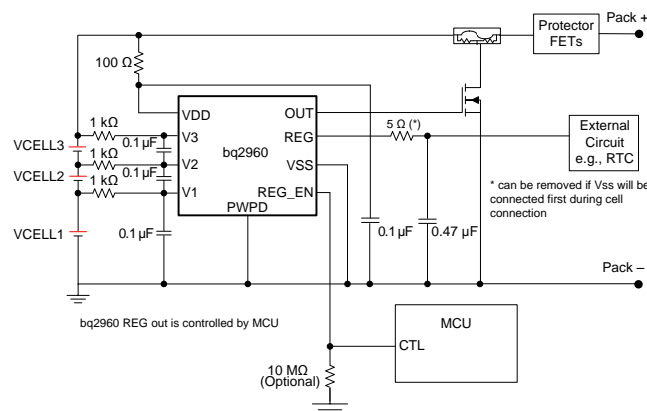
Device Information⁽¹⁾⁽²⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq2960	WSON (8)	2.00 mm \times 2.00 mm
bq2961		
bq2962		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) The bq2960 is a 2-S to 3-S device. The bq2961 and bq2962 are 2-S to 4-S devices.

Simplified Schematic



Copyright © 2017, Texas Instruments Incorporated



Table of Contents

1 Features	1	8.3 Feature Description	12
2 Applications	1	8.4 Device Functional Modes	15
3 Description	1	9 Application and Implementation	18
4 Revision History	2	9.1 Application Information	18
5 Device Comparison Table	4	9.2 Typical Application	18
6 Pin Configuration and Functions	5	10 Power Supply Recommendations	22
7 Specifications	6	11 Layout	22
7.1 Absolute Maximum Ratings	6	11.1 Layout Guidelines	22
7.2 ESD Ratings	6	11.2 Layout Example	22
7.3 Recommended Operating Conditions	6	12 Device and Documentation Support	23
7.4 Thermal Information	6	12.1 Receiving Notification of Documentation Updates	23
7.5 Electrical Characteristics	7	12.2 Community Resources	23
7.6 Typical Characteristics	9	12.3 Trademarks	23
8 Detailed Description	11	12.4 Electrostatic Discharge Caution	23
8.1 Overview	11	12.5 Glossary	23
8.2 Functional Block Diagram	11	13 Mechanical, Packaging, and Orderable Information	23

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2016) to Revision D	Page
Changed device label from "bq2960xy" to "bq2960" and changed device label from "bq2961xy" to "bq2961/bq2962" in the Simplified Schematic	1
Separated bq2961 and bq2962 device options into two tables	4
Removed bq296100 preview status. Added bq296215, bq296216, bq296217 device spins to Device Comparison Table	4
Extended IDD test condition from $(V_n - V_{n-1}) = 3.8V$ to $(V_n - V_{n-1}) = 2V$ to 4.15V	7
Added VOUT TYP and MAX specification	7
Added VREG specification at 500 μA load. Was only specified with 0~1mA range before.	8
Extended IREG MAX specification to 2mA, was 1mA before	8
Changed device label from "bq2960xy" "bq2960" in Application Schematic	15
Corrected REG capaitor to 0.47uF in the current consumption test circuit, was 0.1uF.	17
Changed device label from "bq2961xy" to "bq2961/bq2962" in reference schematic. Updated figure title to "bq2961 and bq2962 schematic", was "bq2961 schematic" before	19
Changed device label from "bq2960xy" to "bq2960" in reference schematic	21
Changed device label from "bq2961xy" to "bq2961/bq2962". Updated figure title to bq2961 and bq2962 schematic	22
Added <i>Receiving Notification of Documentation Updates</i> section	23

Changes from Revision B (May 2016) to Revision C	Page
Added bq2962 REG options	1
Changed Part number to bq2960, bq2961, bq2962 to identify each spin family throughout the datasheet	1
Added bq296202, bq296203, bq296212, bq296213	4
Added bq2962 pinout	5
Added bq2962 device to Recommended Operating Conditions	6
Extended bq2962 VREG full range condition from 0mA to 2mA, was 0mA to 1mA before	8
Added bq2962 regulator programmable option	11
Changed figure title to apply to bq2962 family	19

-
- Changed figure title to apply to bq2962 [22](#)
-

Changes from Revision A (January 2016) to Revision B	Page
---	-------------

- Added bq296114 to [Device Comparison Table](#)..... [4](#)
-

Changes from Original (November 2013) to Revision A	Page
--	-------------

- Changed the device listing in the data sheet header information to: bq2961 [1](#)
 - Changed bq296106, '107, '111 From: Preview To: Released status [4](#)
 - Added bq296112 to [Device Comparison Table](#) [4](#)
 - Added bq296113 to [Device Comparison Table](#)..... [4](#)
 - Added Available the bq2961xy configuration range to [Device Comparison Table](#) [4](#)
-

5 Device Comparison Table

Table 1. bq2962 Device Options

bq2962	OVP (V)	OVP DELAY (s)	UV (V)	LDO (V)
bq296202	4.45	6.5	2.5	3.3
bq296203	4.50	6.5	2.5	3.3
bq296212	4.50	3.0	2.5	3.3
bq296213	4.35	3.0	2.5	3.3
bq296215 ⁽¹⁾	4.50	6.5	2.5	3.0
bq296216	4.55	6.5	2.5	3.0
bq296217	4.55	6.5	2.8	3.3
bq2962	3.85V - 4.60V (50mV step)	3.0, 4.0, 5.5, 6.5	2.0V - 2.8V (50mV step)	3, 3.15, 3.3

(1) Product Preview only

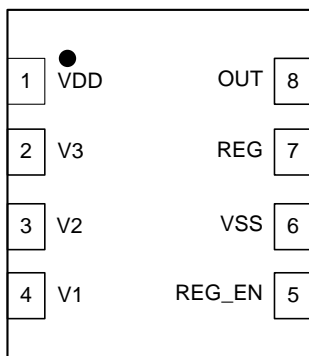
Table 2. bq2961 Device Options

bq2961	OVP (V)	OVP DELAY (s)	UV (V)	LDO (V)
bq296100	4.35	6.5	2.5	3.3
bq296101 ⁽¹⁾	4.40	6.5	2.5	3.3
bq296102 ⁽¹⁾	4.45	6.5	2.5	3.3
bq296103	4.50	6.5	2.5	3.3
bq296104 ⁽¹⁾	4.35	6.5	2.8	3.3
bq296105 ⁽¹⁾	4.40	6.5	2.8	3.3
bq296106	4.45	6.5	2.8	3.3
bq296107	4.50	6.5	2.8	3.3
bq296108 ⁽¹⁾	4.50	6.5	2.4	3.3
bq296109 ⁽¹⁾	4.325	3.0	2.5	3.3
bq296110 ⁽¹⁾	4.45	3.0	2.5	3.3
bq296111	4.45	4.0	2.5	3.3
bq296112	4.50	3.0	2.5	3.3
bq296113	4.35	3.0	2.5	3.3
bq296114	4.50	4.0	2.5	3.3
bq2961	3.85V - 4.60V (50mV step)	3.0, 4.0, 5.5, 6.5	2.0V - 2.8V (50mV step)	1.8, 2.5, 3.3

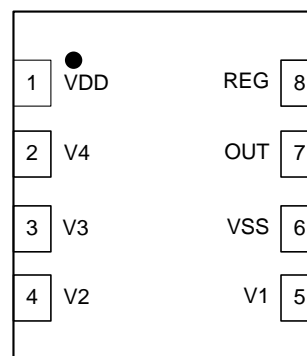
(1) Product Preview only

6 Pin Configuration and Functions

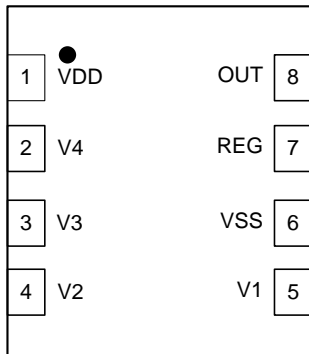
**2s-to-3s bq2960
(Top View)**



**2s-to-4s bq2962
(Top View)**



**2s-to-4s bq2961
(Top View)**



Pin Functions

PIN				TYPE ⁽¹⁾	DESCRIPTION
NAME	bq2960	bq2961	bq2962		
OUT	8	8	7	OA	Analog Output drive for overvoltage fault signal, CMOS Output High or Open Drain Active Low.
PWPD	9	9	9	P	TI recommends connecting the exposed pad to VSS on PCB.
REG	7	7	8	OA	Regulated Supply Output. Requires an external ceramic capacitor for stability.
REG_EN	5	—	—	IA	Regulated Supply Output Enable. A "high" to enable REG output and "low" to disable REG output.
V1	4	5	5	IA	Sense input for positive voltage of the lowest cell from the bottom of the stack.
V2	3	4	4	IA	Sense input for positive voltage of the second cell from the bottom of the stack.
V3	2	3	3	IA	Sense input for positive voltage of the third cell from the bottom of the stack.
V4	—	2	2	IA	Sense input for positive voltage of the fourth cell from the bottom of the stack.
VDD	1	1	1	P	Power supply input
VSS	6	6	6	P	Electrically connected to integrated circuit ground and negative terminal of the lowest cell in the stack.

(1) IA = Analog input, OA = Analog Output, P = Power connection

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	VDD – VSS	–0.3	30	V
Input voltage	V4 – V3, V3 – V2, V2 – V1, V1 – VSS	–0.3	30	
	REG – VSS	–0.3	3.6	
	REG_EN – VSS	–0.3	28	
Output voltage	OUT – VSS	–0.3	30	
Continuous total power dissipation, P _{TOT}		See Thermal Information .		
Lead temperature (soldering, 10 s), T _{SOLDER}		300	300	°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Procedures](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage, V _{DD} ⁽¹⁾	Supply voltage, V _{DD} ⁽¹⁾ , bq2960	3		15	V
	Supply voltage, V _{DD} ⁽¹⁾ , bq2961, bq2962	3		20	
	Supply voltage, V _{DD} with REG output on	4			
Input voltage range	V _n – V _{n-1} , V1 – VSS	0		5	V
	REG_EN	0		15	V
Operating ambient temperature range, T _A		–40		110	°C

- (1) See [Typical Application](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		bq2960xy	UNIT
		DSG (WSON)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	62	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	72	°C/W
R _{θJB}	Junction-to-board thermal resistance	32.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	33	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	10	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 14.4\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to $+110^\circ\text{C}$, and $V_{DD} = 3\text{ V}$ to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Voltage Protection Thresholds							
V _{OV}	V ^(PROTECT) Overvoltage Detection	R _{IN} = 1 kΩ		Applicable Voltage: 3.85 V to 4.6 V in 50 mV steps			V
V _{HYS}	OV Detection Hysteresis			250	300	400	mV
V _{OA}	OV Detection Accuracy	T _A = 25°C		−10		10	mV
V _{OADRIFT}	OV Detection Accuracy Across Temperature	T _A = −40°C		−40		40	mV
		T _A = 0°C		−20		20	mV
		T _A = 60°C		−24		24	mV
		T _A = 110°C		−54		54	mV
		T _A = 110°C		−54		54	mV
Supply and Leakage Current							
I _{DD}	Supply Current with REG on	(V _n − V _{n-1}) = 2 V to 4.15 V, n = 1 to 4, VDD = top V _n voltage (V1 − V _{SS}) > V _{UVREG} , I _{REG} = 0 mA,	T _A = 0°C to 60°C		4	6	μA
			T _A = −40°C to 110°C			8	μA
I _{DD}	Supply Current with REG off	(V _n − V _{n-1}) = 2 V to 4.15 V, n = 1 to 4, VDD = top V _n voltage (V1 − V _{SS}) < V _{UVREG}	T _A = 0°C to 60°C		1	2	μA
			T _A = −40°C to 110°C			4	μA
I _{IN}	Input Current at V _x Pins	(V _n − V _{n-1}) = (V1 − V _{SS}) = 3.8 V, VDD = top V _n voltage, T _A = 25°C		−0.1		0.1	μA
Output Drive OUT, CMOS Active High							
V _{OUT}	Output Drive Voltage, Active High	(V _n − V _{n-1}) or (V1 − V _{SS}) > V _{OV} , I _{OH} = 100 μA, VDD = top V _n voltage		6	7	8	V
		If three of four cells are short circuited, only one cell remains powered and > V _{OV} , VDD = V _n (the remaining cell voltage), I _{OH} = 100 μA			VDD − 0.3		V
		(V _n − V _{n-1}) and (V1 − V _{SS}) < V _{OV} , VDD = sum of the cell stack voltage, I _{OL} = 100 μA measured into OUT pin			250	400	mV
I _{OUTH}	OUT Source Current (during OV)	(V _n − V _{n-1}), (V3 − V2), or (V1 − V _{SS}) > V _{OV} , VDD = top V _n voltage, forced OUT = 0 V, measured out of OUT pin				4.5	mA
I _{OUTL}	OUT Sink Current (no OV)	(V _n − V _{n-1}) and (V1 − V _{SS}) < V _{OV} , VDD = top V _n voltage, forced OUT = VDD, measured into OUT pin. Pull-up resistor R _{PU} = 5 kΩ to VDD		0.5		14	mA
Internal Fixed Delay Timer							
t _{DELAY}	OV Delay Time ⁽¹⁾	Internal Fixed Delay, 3 second delay option		2.4	3	3.6	s
		Internal Fixed Delay, 4 second delay option		3.2	4	4.8	s
		Internal Fixed Delay, 5.5 second delay option		4.4	5.5	6.6	s
		Internal Fixed Delay, 6.5 second delay option		5.2	6.5	7.8	s
t _{DELAY_CTM}	Fault Detection Delay Time in Test Mode OV Delay Time	Internal Fixed delay			15		ms

(1) Specified by design. Not 100% tested in production.

Electrical Characteristics (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 14.4\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to $+110^\circ\text{C}$, and $V_{DD} = 3\text{ V}$ to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Regulated Supply Output, REG							
V _{REG}	REG Supply at 500 μA load	V _{DD} ≥ 4 V, I _{REG} = 500 μA, C _{REG} = 0.47 μF	V _{REG} = 3.3 V , bq2960, bq2961, bq2962	3.234	3.300	3.366	V
			V _{REG} = 3.15 V , bq2962	3.087	3.150	3.213	
			V _{REG} = 3.0 V , bq2962	2.940	3.000	3.060	
			V _{REG} = 2.5 V , bq2960, bq2961	2.450	2.500	2.550	
			V _{REG} = 1.8 V , bq2960, bq2961	1.764	1.800	1.836	
V _{REG}	REG Supply from 0 to 2 mA load	V _{DD} ≥ 4 V, I _{REG} = 0 μA to 2 mA, C _{REG} = 0.47 μF	V _{REG} = 3.3 V , bq2960, bq2961, bq2962	3.200	3.300	3.400	V
			V _{REG} = 3.15 V , bq2962	3.050	3.150	3.250	
			V _{REG} = 3.0 V , bq2962	2.900	3.000	3.100	
			V _{REG} = 2.5 V , bq2960, bq2961	2.425	2.500	2.575	
			V _{REG} = 1.8 V , bq2960, bq2961	1.746	1.800	1.854	
I _{REG}	REG Current Output	V _{DD} ≥ 4 V, C _{REG} = 0.47 μF	0		2	mA	
I _{REG_SC_Limit}	REG Output Short Circuit Current Limit	REG = V _{SS} , C _{REG} = 0.47 μF	4			mA	
R _{REG_PD}	REG pull-down resistor	REG is disabled	20	30	45	kΩ	
Regulated Supply Output Enable, REG_EN							
V _{IH}	High-level Input		1.6			V	
V _{IL}	Low-level Input				0.4	V	
I _{LKG}	Input Leakage Current	V _{IH} < 6 V			0.1	μA	
Regulated Supply Undervoltage Self-disable							
V _{UVREG}	Undervoltage detection	Factory Configuration: 2.0 V to 2.8 V in 50 mV steps, T _A = 25 °C	–50		50	mV	
V _{UVHYS}	Undervoltage Detection Hysteresis		250	300	400	mV	
t _{UVDELAY}	Undervoltage Detection Delay		4.5	6	7.5	s	
V _{UVQUAL}	Cell voltage to qualify for UV detection			0.5		V	

7.6 Typical Characteristics

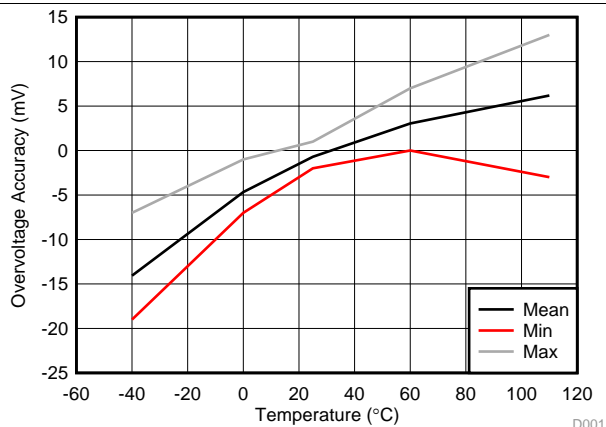


Figure 1. Overvoltage Threshold (V_{OV}) vs Temperature

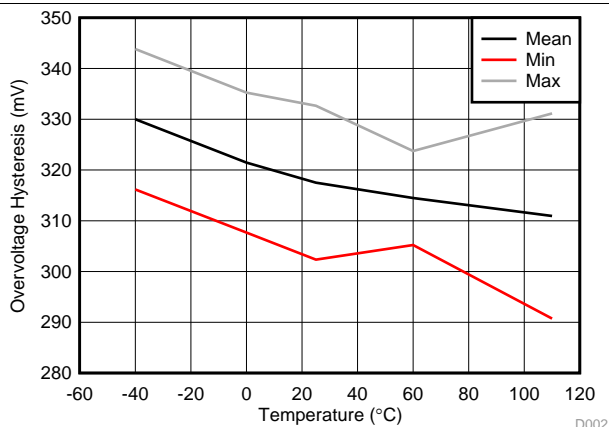


Figure 2. Hysteresis V_{HYS} vs Temperature

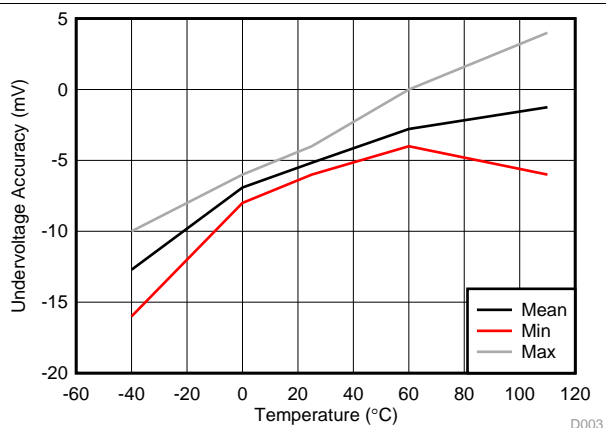


Figure 3. Undervoltage Accuracy

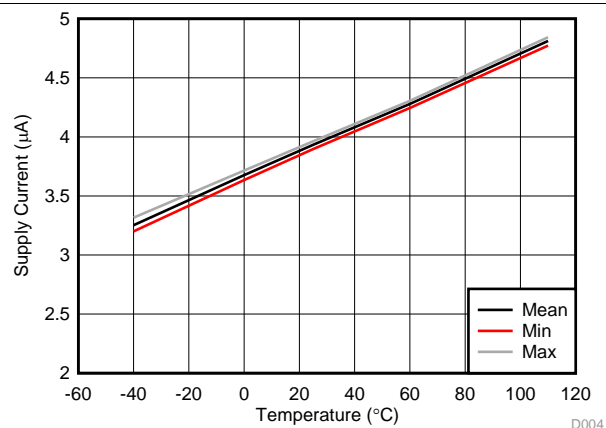


Figure 4. I_{DD} with Regulator On

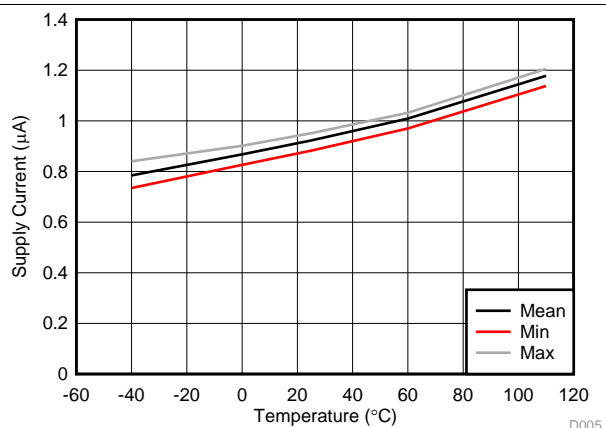


Figure 5. I_{DD} with Regulator Off

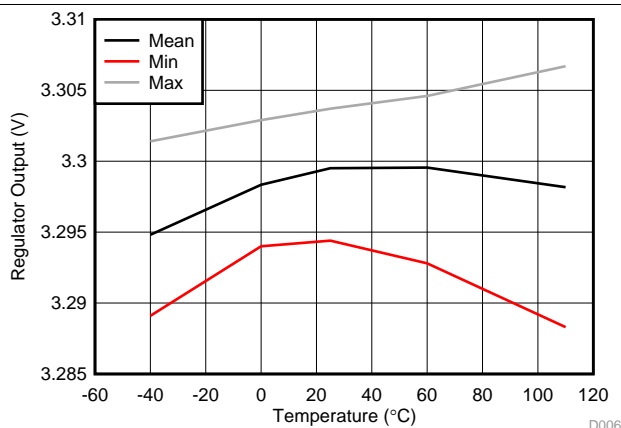


Figure 6. Regulator Output Without Load

Typical Characteristics (continued)

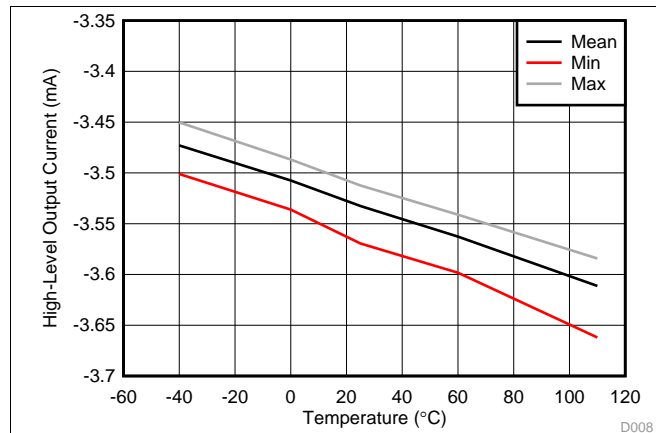


Figure 7. I_{OUTH} vs Temperature

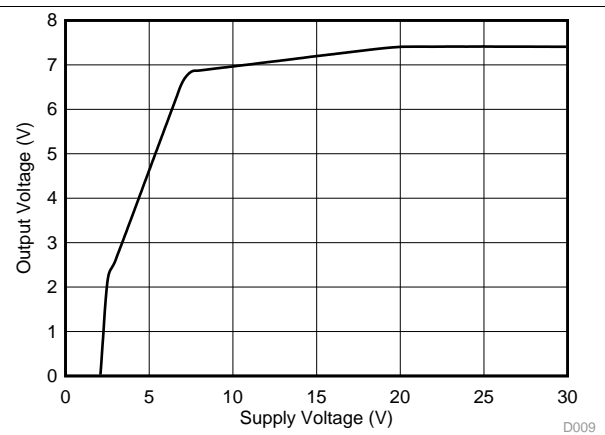


Figure 8. V_{OUT} vs V_{DD}

8 Detailed Description

8.1 Overview

The bq2960, bq2961 and bq2962 are second-level overvoltage (OV) protectors with a regulated output. Each cell is monitored independently by comparing the actual cell voltage to an overvoltage threshold V_{OV} . The overvoltage threshold is preprogrammed at the factory with a range between 3.85 V to 4.65 V.

The regulated output is enabled unless any of the cell voltages fall below the V_{UVREG} threshold. This threshold is preprogrammed at the factory with a range between 2 V to 2.8 V. For bq2960xy family, an external control pin, REG_EN, is available to enable or disable the regulated output in addition to the V_{UVREG} detection.

Table 3. Programmable Parameters

OVERVOLTAGE RANGE (V)	OVERVOLTAGE DELAY (s)	UNDERVOLTAGE RANGE (V)	REGULATOR (V)
3.85 to 4.6 in 50 mV step	3, 4, 5.5, 6.5	2.0 to 2.8 in 50 mV step	1.8, 2.5, 3.3 (bq2960, bq2961) 3.0, 3.15, 3.3 (bq2962)

8.2 Functional Block Diagram

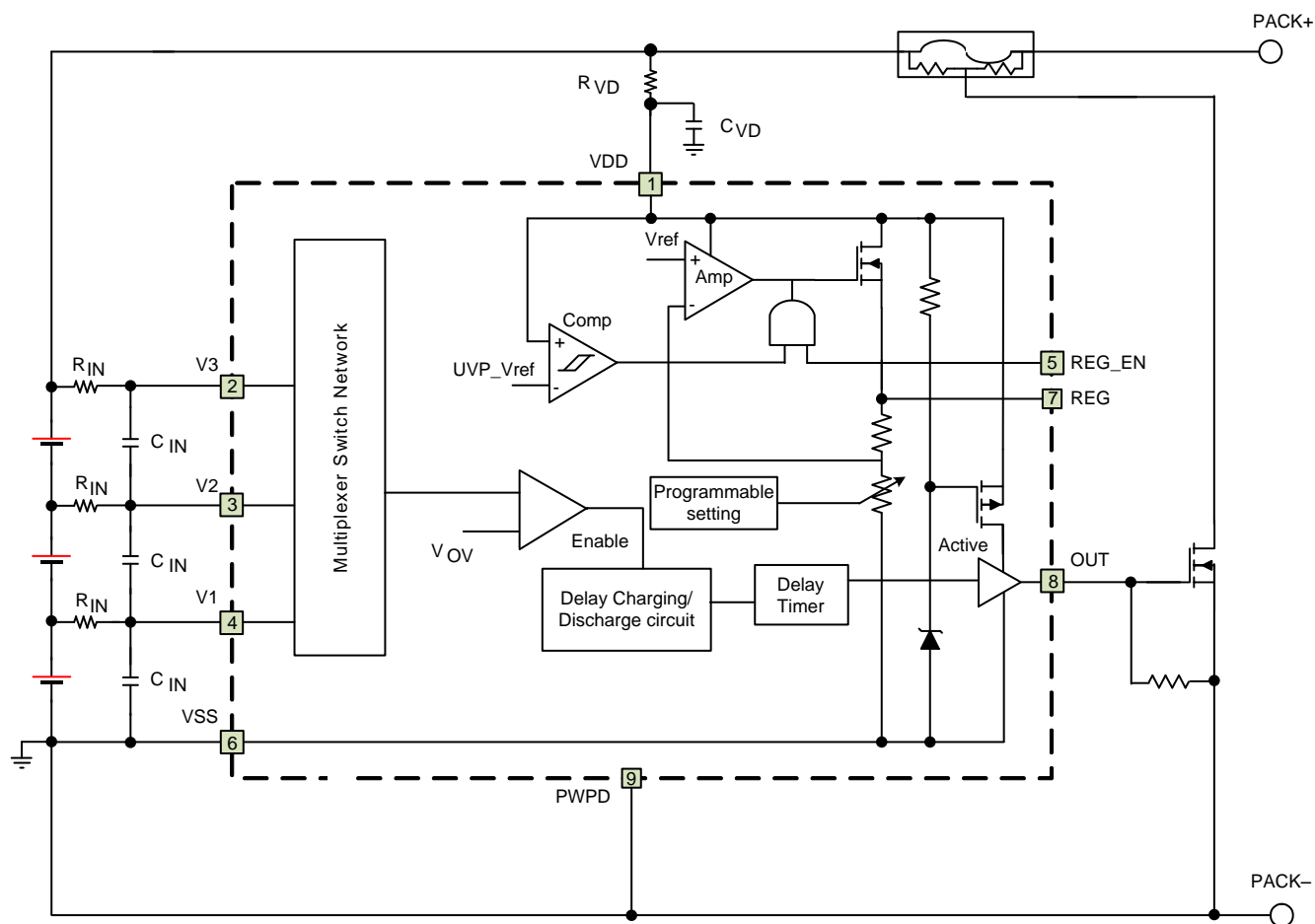


Figure 9. bq2960 Block Diagram

Functional Block Diagram (continued)

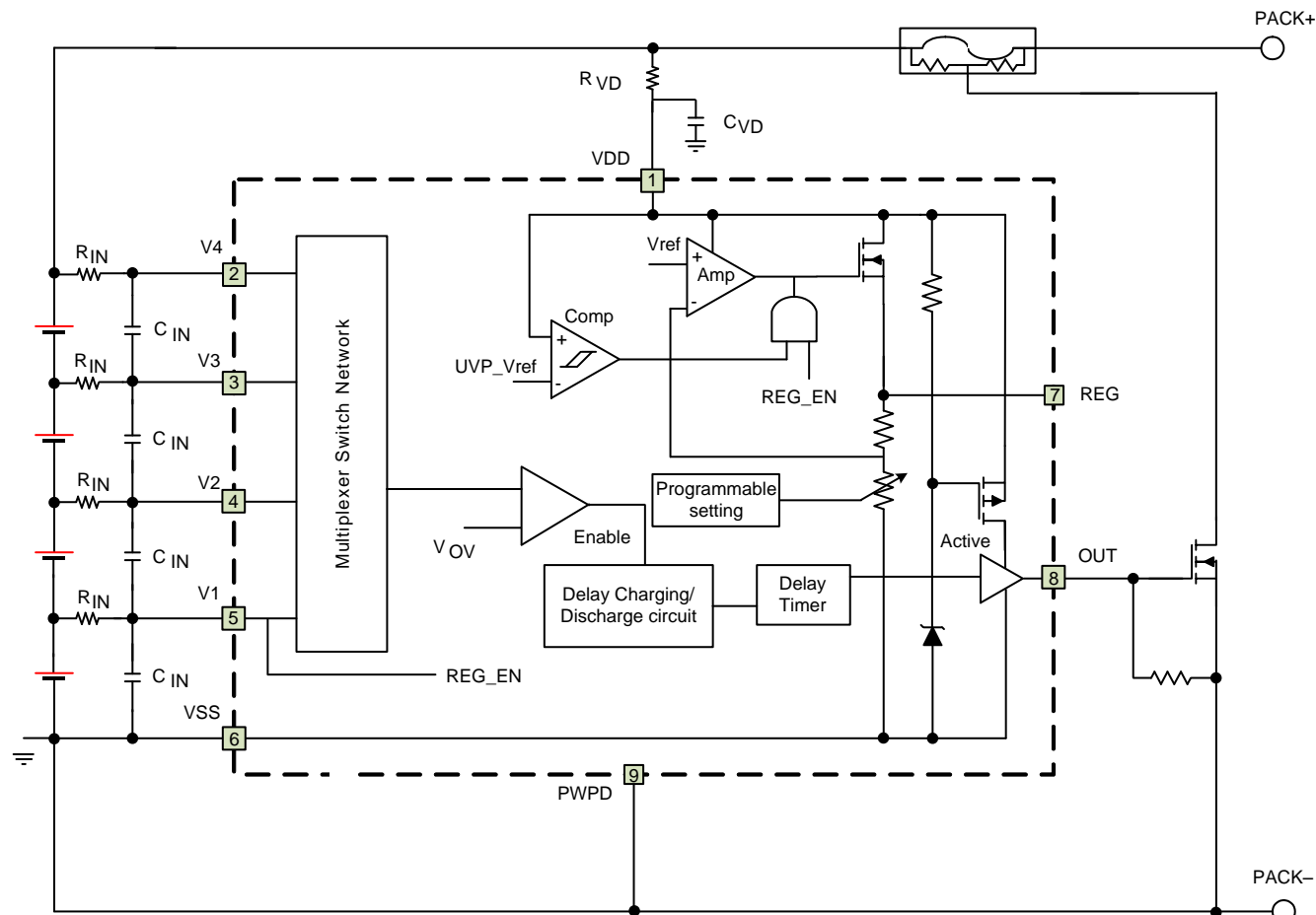


Figure 10. bq2961 and bq2962 Block Diagram

8.3 Feature Description

8.3.1 Pin Details

8.3.1.1 Input Sense Voltage, V_x

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.1.2 Output Drive, OUT

This terminal serves as the fault signal output in Active High.

8.3.1.3 Supply Input, VDD

This terminal is the unregulated input power source for the device. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.1.4 Regulated Supply Output, REG

This terminal is connected to an external capacitor and provides a regulated supply to power a circuit such as a Real Time Clock integrated circuit, or functions requiring a well-regulated supply. Maximum current load on this pin cannot exceed 1 mA.

Feature Description (continued)

The REG output has protection for overcurrent, using a current limit protection circuit, and also detects and protects for excessive power dissipation due to short circuit of the external load. This pin requires a ceramic 1- μ F capacitor connection to VSS for improved stability, noise immunity, and ESD performance of the supply output. This capacitor must be placed close to the REG and VSS pins for connection.

8.3.1.5 Regulated Supply Output Enable, REG_EN (bq2960 Only)

This terminal is a high voltage input drain to enable and disable the regulated supply output, REG terminal. When the VREG_EN > V_{IH} , the REG terminal output is enabled including the cell undervoltage detection function to self-disable the regulated supply. When the VREG_EN < V_{IL} , the REG terminal output, the cell undervoltage detection and the regulated supply self-disable functions are disabled.

To keep the REG output enabled at all times, the recommendation is to connect the REG_EN to the V1 termination. There is a 6-V clamp to protect the REG_EN terminal from a high voltage input. By connecting REG_EN to V1, the clamp circuit is not active.

When the REG output is enabled, VREG_EN > V_{IH} , the REG output can be self-disabled if any of the cell voltages are < V_{UVREG} . The self-disable function is used to reduce power consumption when the battery pack is deeply depleted.

8.3.2 Overvoltage Sensing for OUT

In the bq296xxx device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV} . If any cell voltage exceeds the programmed OV value, an internal timer circuit is activated. This timer circuit causes a factory pre-programmed fixed delay before the OUT terminal goes from inactive to active state.

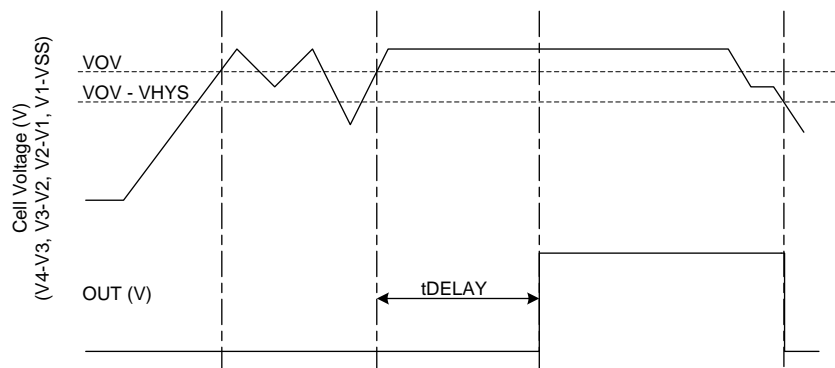


Figure 11. Timing for Overvoltage Sensing for OUT

8.3.3 Regulated Output Voltage and REG_EN Pin

For bq2960 and bq2961, there are three factory-preprogrammed options for the regulated output voltage, 3.3 V, 2.5 V, and 1.8 V. For bq2962, the regulated output voltage options are 3.3 V, 3.15 V, and 3.0 V. bq2962xy can potentially provide other regulated voltage output between 3.3 V to 3.0 V, contact Texas Instruments for detail.

At power up, the regulated output is on by default. If any cell voltage is below V_{UVREG} at device power up, the regulated output will remain on until the t_{UV_DELAY} time has passed, the regulated out turns off after the delay time.

During discharge, if any cell voltage falls below the V_{UVREG} threshold for t_{UV_DELAY} time, the regulated output is self-disabled. The regulated output turns on again when all the cell voltages are above $V_{UVREG} + V_{UVHYS}$.

Feature Description (continued)

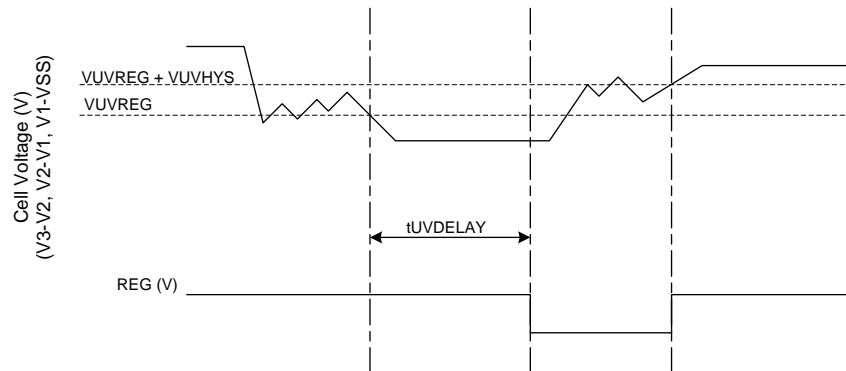


Figure 12. REG Output Timing

For bq2960 family, an external REG_EN pin is available to enable and disable the regulated output function. To enable both the regulated output and the undervoltage self-disable features, the REG_EN pin must be above V_{IH} . A microcontroller can be used to control the REG_EN pin. Alternatively, connecting the REG_EN pin to the bottom cell is another option to enable the regulated output function always.

Feature Description (continued)

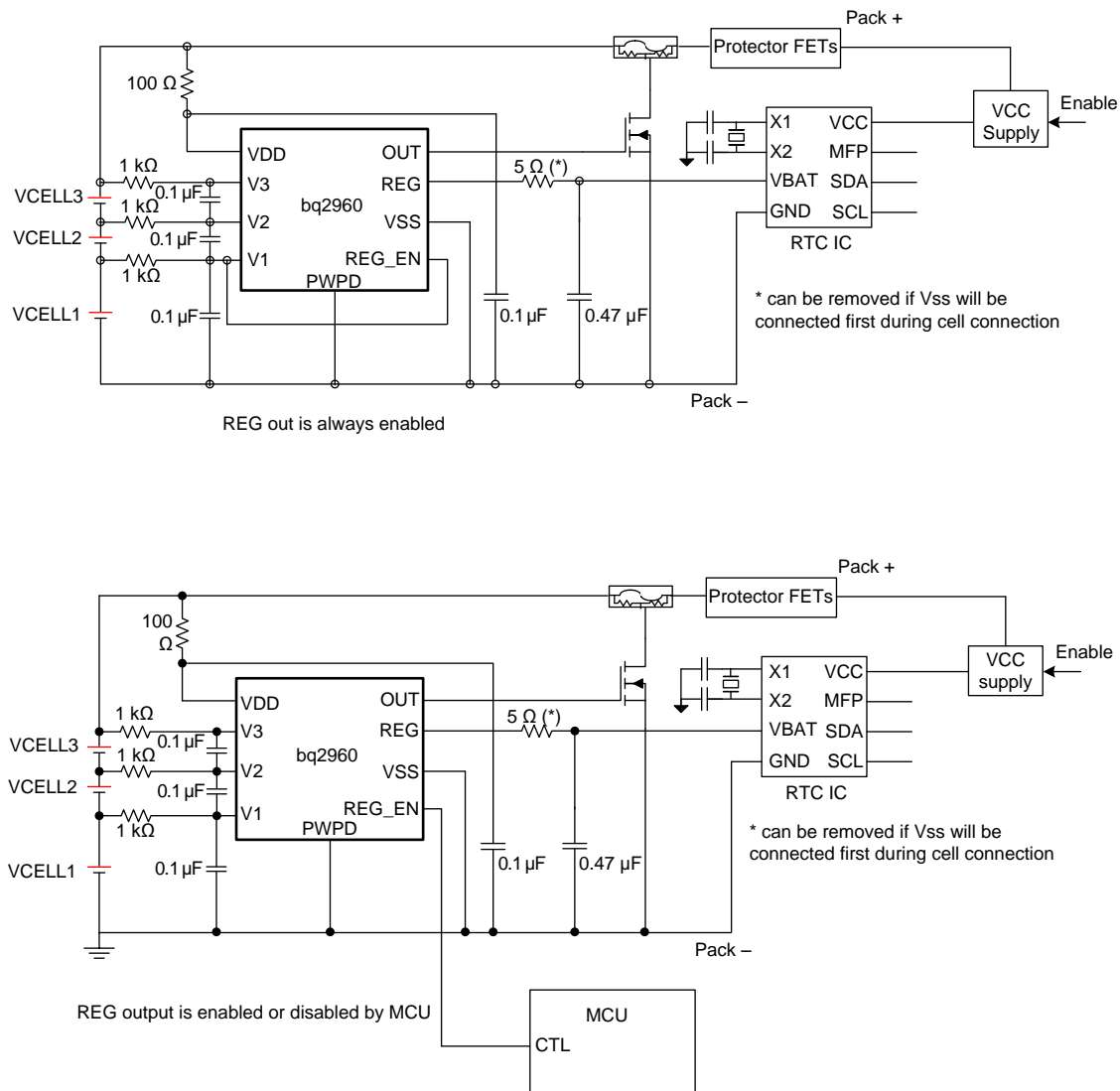


Figure 13. bq2960 Application Schematic

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the V_{OV} threshold AND above V_{UVREG} threshold, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1), (V3–V2), and (V4–V3). The OUT pin is inactive in this mode. The regulated output is always enabled for bq2961. For bq2960, the regulated output is on only if the voltage on the REG_EN pin is above V_{IH} .

Device Functional Modes (continued)

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceed the overvoltage threshold, V_{OV} , for configured OV delay time. The OUT pin is activated after a delay time preprogrammed at the factory. The OUT pin will pull high internally. Then an external FET is turned on, shorting the fuse to ground, which allows the battery and/or charger power to blow the fuse. When all of the cell voltages fall below $(V_{OV} - V_{HYS})$, the device returns to NORMAL mode. The regulated output (if enabled) remains on in this mode.

8.4.3 UNDERVOLTAGE Mode

The UNDERVOLTAGE mode is detected if any of the cell voltage across $(V1-VSS)$, $(V2-V1)$, $(V3-V2)$, or $(V4-V3)$ is below the V_{UVREG} threshold for t_{UV_DELAY} time. In this mode, the regulated output is disabled. To return to the NORMAL mode, all the cell voltages must be above $(V_{UVREG} + V_{UVHYS})$.

For a low cell configuration, V_n pin can be shorted to the $(V_n - 1)$ pin. The device ignores any differential cell voltage below V_{UVQUAL} threshold for undervoltage detection.

8.4.4 CUSTOMER TEST MODE

The Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay-timer parameter once the circuit is implemented into the battery pack. To enter CTM, the VDD pin should be set at least 10 V higher than V3 (see Figure 14). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to VC3 voltage differential of 10 V, so that the decrease in the value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the device into CTM. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages $(V3-V2)$, $(V2-V1)$ and $(V1-VSS)$. Stressing the pins beyond the rated limits can cause permanent damage to the device.

Figure 14 shows the timing for the Customer Test Mode.

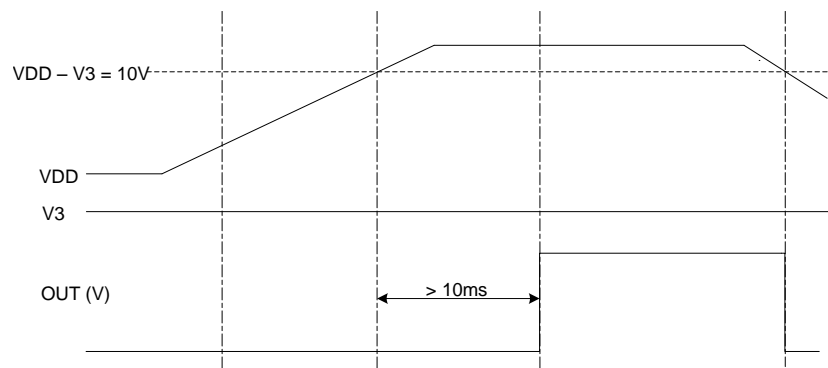


Figure 14. Timing for Customer Test Mode

Device Functional Modes (continued)

Figure 15 shows the measurement for current consumption of the product for both VDD and Vx.

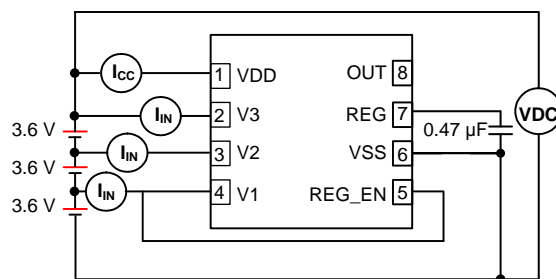


Figure 15. Configuration for Integrated Circuit Current Consumption Test

9 Application and Implementation

NOTE

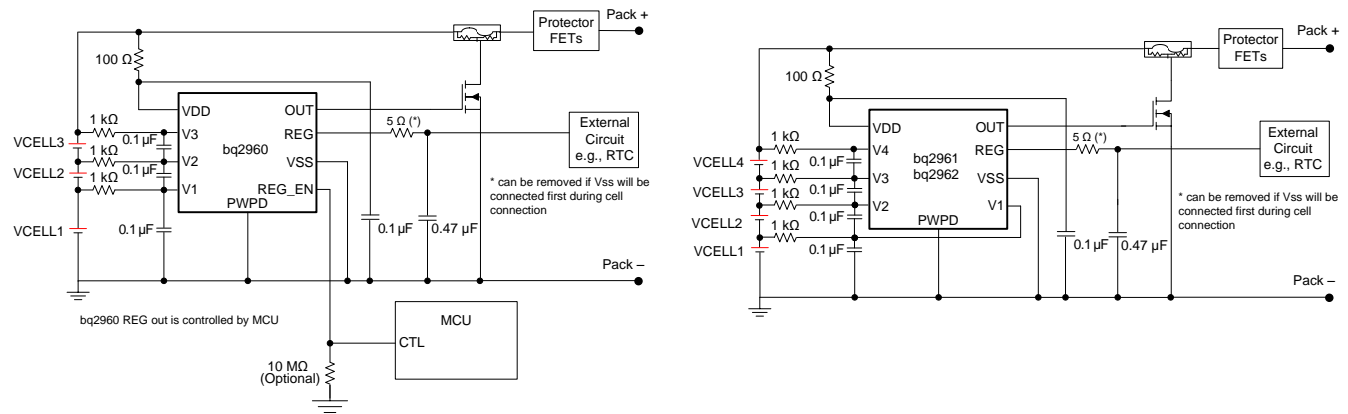
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq296xxx is a family of second-level protectors used for overvoltage protection of the battery pack in the application. A regulated output is available to drive a small circuit with maximum I_{REG} loading. The device OUT pin is active high, which drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery and/or charger power to blow the fuse and cut the power path.

9.2 Typical Application

Figure 13 shows the recommended reference design components.



Copyright © 2017, Texas Instruments Incorporated

Figure 16. Application Schematic

9.2.1 Design Requirements

NOTE

Changes to the ranges stated in Table 4 will impact the accuracy of the cell measurements.

Table 4. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	4700	Ω
Voltage monitor filter capacitance	C_{IN}	0.01	0.1	1.0	μF
Supply voltage filter resistance	R_{VD}	0.1	—	1	$K\Omega$
Supply voltage filter capacitance	C_{VD}	—	0.1	1.0	μF
REG output capacitance	C_{REG}	0.47	1	—	μF

NOTE

The device is calibrated using an R_{IN} value = 1 k Ω . Using a value other than the recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

9.2.2 Detailed Design Procedure

NOTE

The device VSS must be connected first during PCB test or cell attachment. Failure to do so can damage the REG pin.

1. If VSS pin cannot be connected first, it is required to add a resistor of a minimum of 5 ohms to a maximum of 10 ohms (a 5-ohm resistor is used in the reference schematic, [Figure 17](#)) in series with the REG capacitor. When VSS is floating, the REG capacitor always charges up to the VDD voltage. When VSS is finally connected, the REG capacitor will be discharged. Adding a small resistor in series reduces the current strength and avoids any potential damage to the REG pin. The 5-ohm resistor can be placed in series with the REG connect circuit (as shown in [Figure 17](#)) or in series of the REG capacitor (as shown in [Figure 18](#)). Placing the resistor in series with the REG circuit results in a small drop of VREG (for example: max loading of 1 mA with a 5-ohm resistor will drop 5 mV on VREG), but such a connection can protect against rush current discharge from both REG capacitor or external filter capacitor connected to the REG pin. Placing the resistor in series with the REG capacitor is an alternative to avoid additional drop in VREG if the filter capacitor used by the external circuit is much smaller than the REG capacitor.
2. After VSS is connected, the device allows random cell connect to the Vx pin.
3. Cell should be connected to the lower V_n pin; the unused V_n pin should be shorted to the (V_{n-1}) pin. See [Figure 17](#) for details.

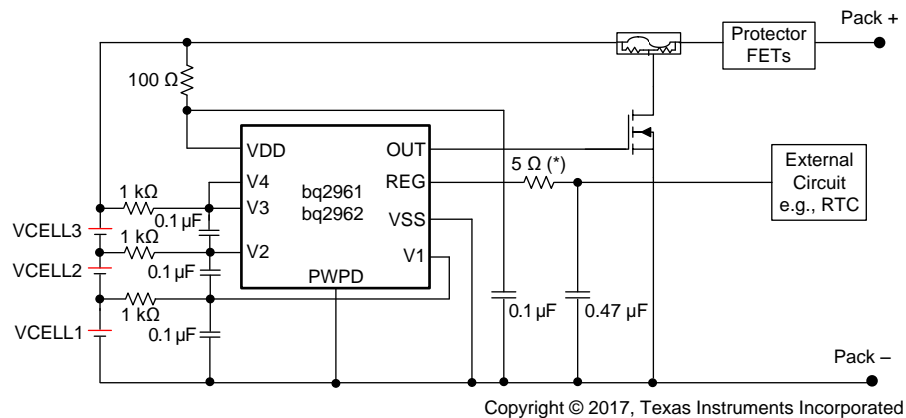


Figure 17. 3-Series bq2961 and bq2962 Schematic

4. A zener diode can be added to the REG pin to VSS as shown in [Figure 18](#). This is recommended to protect the circuit connected to the REG pin if floating VSS in the field is a risk concern. When VSS is floating (during cell connection when VSS is not connected first or in system fault with BAT– wire broken), the REG voltage always pulls up to VDD. In a 4-S configuration, the REG voltage can reach approximately 16 V with VSS floating. Adding a zener diode clamps the REG voltage to a safe level for the external circuits connected to the REG pin. Having the zener diode can also protect the external circuits if REG pin is shorted to OUT pin or any other high-voltage output terminal. If a zener diode is used, TI recommends putting the diode on the battery side with the bq296xxx device to allow protection on both the REG pin as well as the circuit connected to REG under floating VSS condition. The resistor in series with the REG pin is not required in this case.

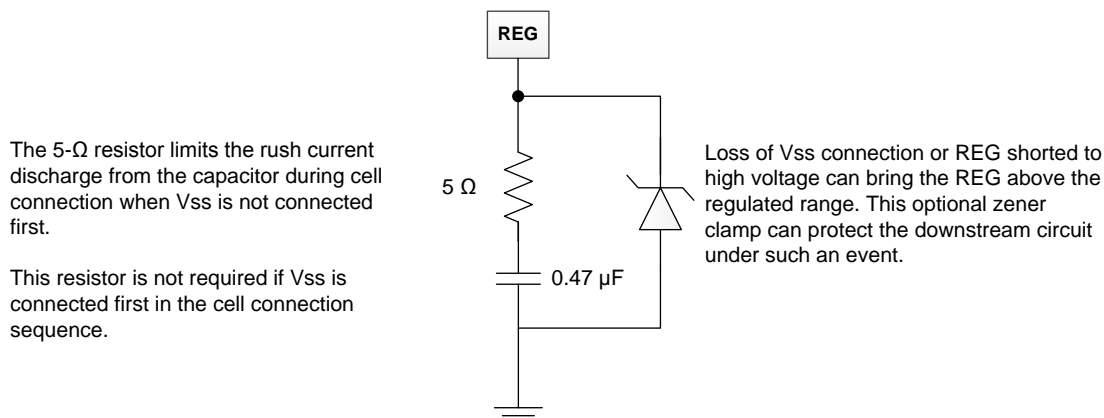


Figure 18. 5-V Zener Diode

- For 2- to 3-series applications, if an external control for the regulated output is required, select the bq2960xy family. Otherwise, select the bq2961xy family.

9.2.3 Application Curves

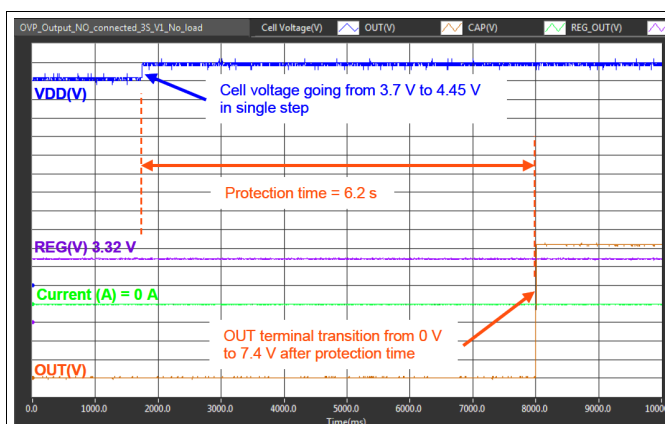


Figure 19. Overvoltage Protection

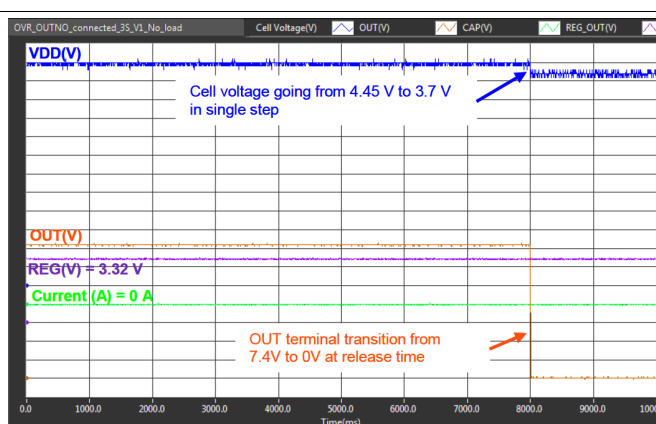


Figure 20. Overvoltage Protection Release

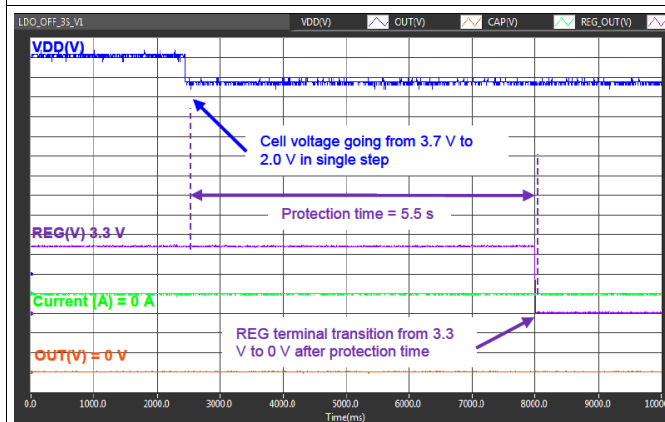


Figure 21. Undervoltage Detection to Turn off Regulator

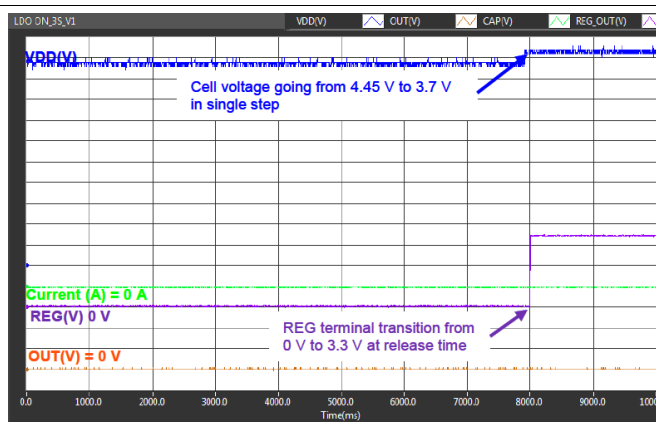
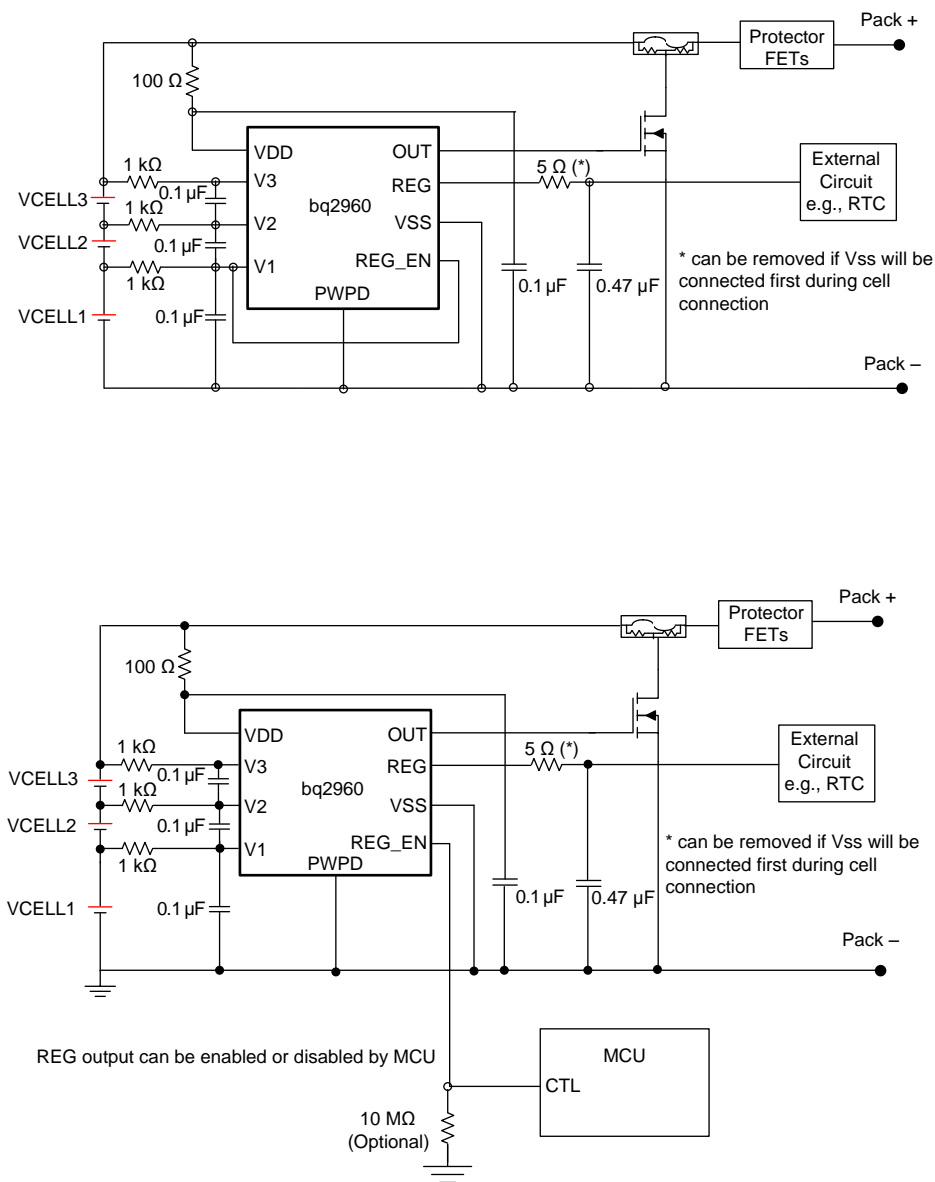


Figure 22. Undervoltage Release to Switch on Regulator

9.2.4 Other Schematics



Copyright © 2017, Texas Instruments Incorporated

Figure 23. bq2960 Schematic with REG Output Always Enabled

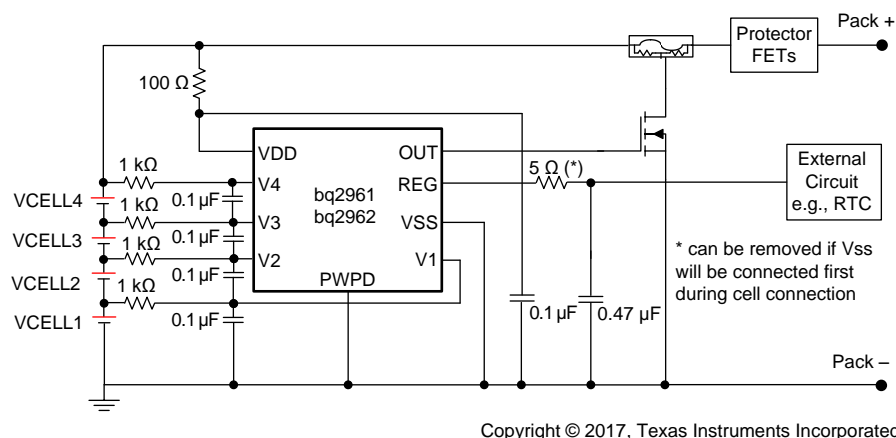


Figure 24. bq2961 and bq2962 Schematic

10 Power Supply Recommendations

The maximum power is 15 V for bq2960 and 20 V for bq2961 and bq2962 on VDD.

NOTE

Connect VSS first during power up.

11 Layout

11.1 Layout Guidelines

Use the following layout guidelines.

1. Ensure the RC filters for the Vx pins and VDD pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for REG should be placed close to the device terminals.
3. Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack- is sufficient to withstand the current during a fuse blown event.

11.2 Layout Example

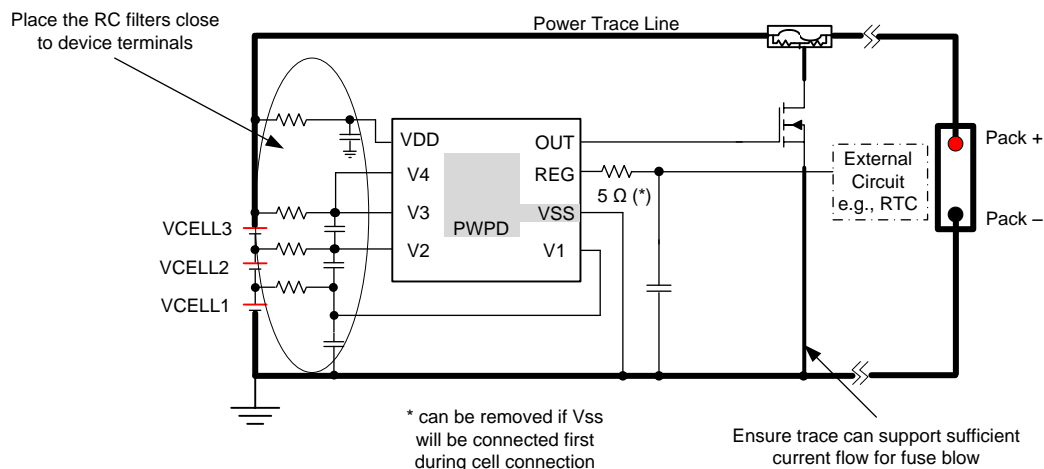


Figure 25. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296100DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6100	Samples
BQ296100DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6100	Samples
BQ296103DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	Samples
BQ296103DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	Samples
BQ296106DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	Samples
BQ296106DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	Samples
BQ296107DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	Samples
BQ296107DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	Samples
BQ296111DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	Samples
BQ296111DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	Samples
BQ296112DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	Samples
BQ296112DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	Samples
BQ296113DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	Samples
BQ296113DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	Samples
BQ296114DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6114	Samples
BQ296114DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6114	Samples
BQ296202DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6202	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296202DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6202	Samples
BQ296203DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6203	Samples
BQ296203DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6203	Samples
BQ296212DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6212	Samples
BQ296212DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6212	Samples
BQ296213DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6213	Samples
BQ296213DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6213	Samples
BQ296216DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6216	Samples
BQ296216DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6216	Samples
BQ296217DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6217	Samples
BQ296217DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6217	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

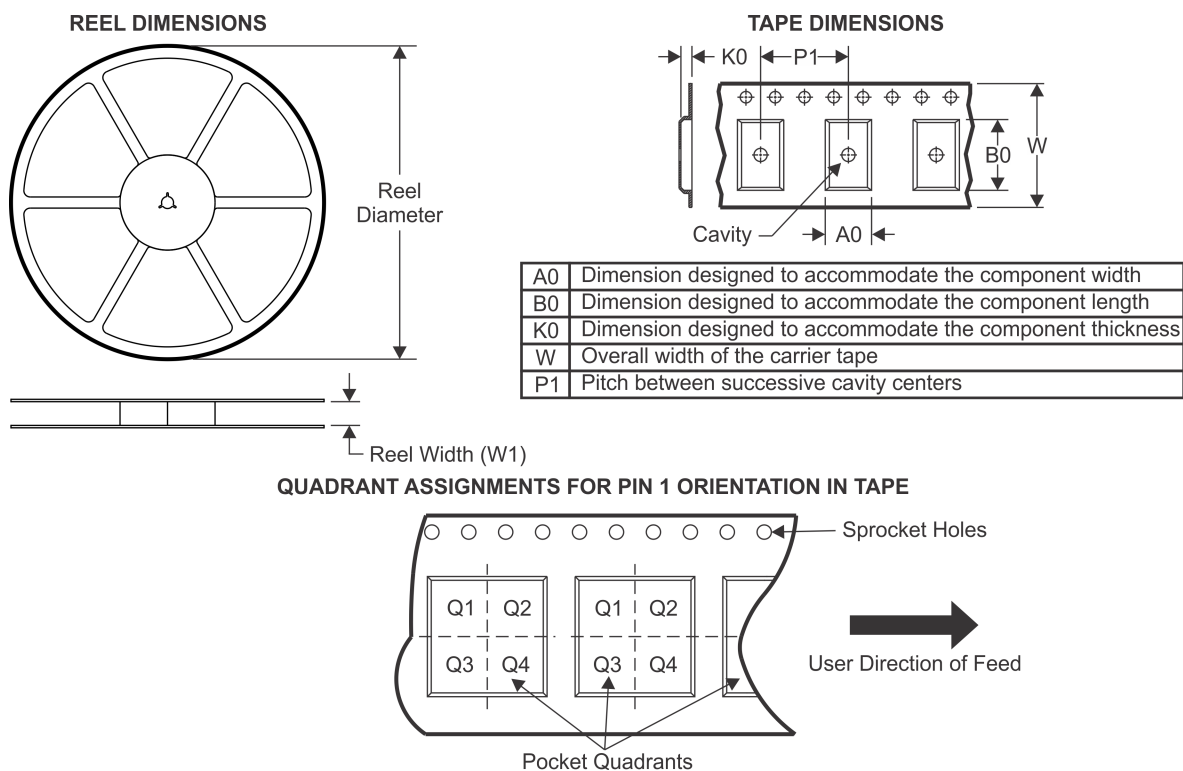
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

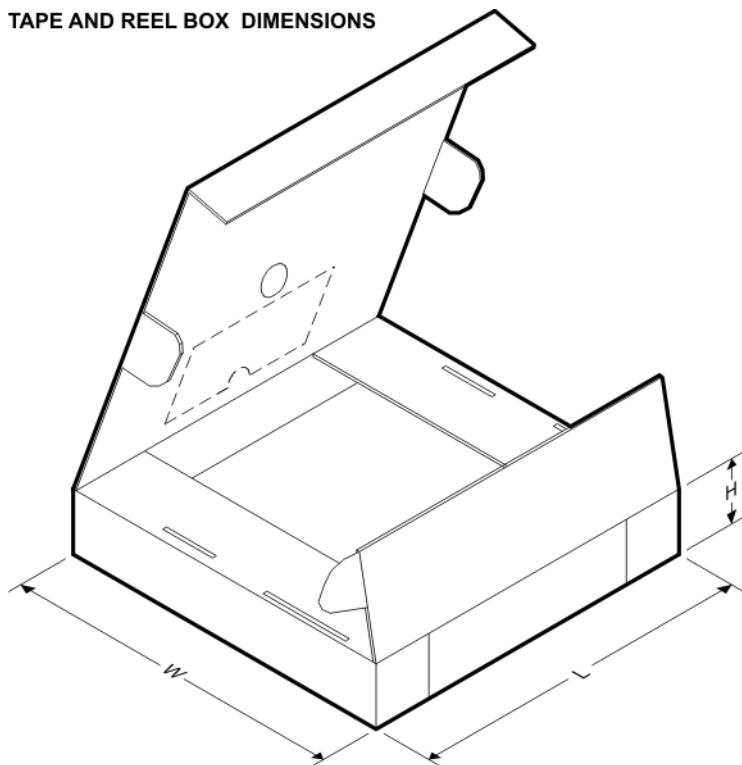
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296100DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296100DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296111DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296111DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296112DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296112DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296113DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296113DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296114DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296114DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296203DSGR	WSN	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296203DSGT	WSN	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296212DSGR	WSN	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296212DSGT	WSN	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296213DSGR	WSN	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296213DSGT	WSN	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296216DSGR	WSN	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296216DSGT	WSN	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296217DSGR	WSN	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296217DSGT	WSN	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


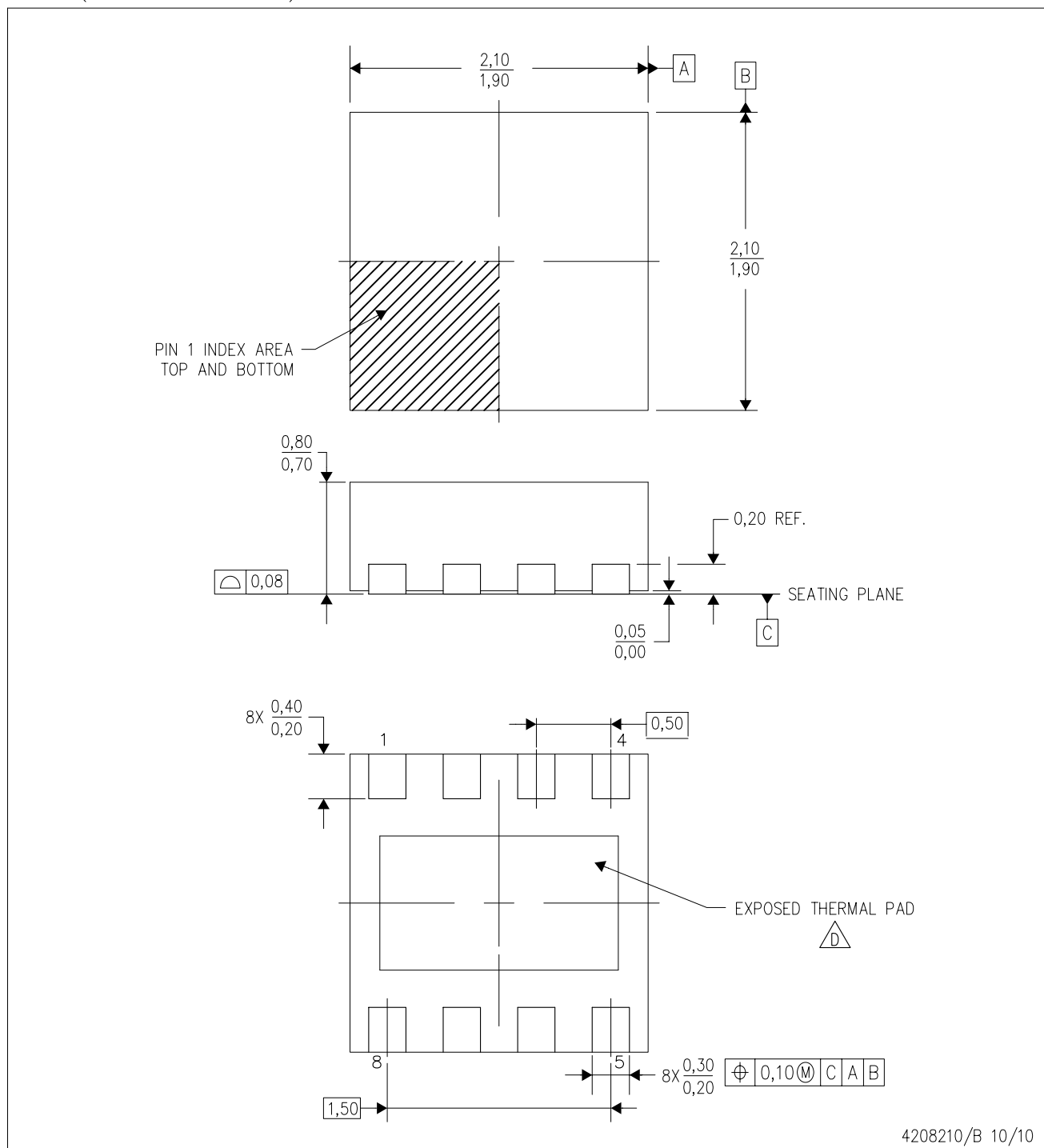
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296100DSGR	WSN	DSG	8	3000	210.0	185.0	35.0
BQ296100DSGT	WSN	DSG	8	250	210.0	185.0	35.0
BQ296103DSGR	WSN	DSG	8	3000	210.0	185.0	35.0
BQ296103DSGT	WSN	DSG	8	250	210.0	185.0	35.0
BQ296106DSGR	WSN	DSG	8	3000	210.0	185.0	35.0
BQ296106DSGT	WSN	DSG	8	250	210.0	185.0	35.0
BQ296107DSGR	WSN	DSG	8	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296107DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296111DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296111DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296112DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296112DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296113DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296113DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296114DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296114DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296202DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296202DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296203DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296203DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296212DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296212DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296213DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296213DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296216DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296216DSGT	WSO	DSG	8	250	210.0	185.0	35.0
BQ296217DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
BQ296217DSGT	WSO	DSG	8	250	210.0	185.0	35.0

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4208210/B 10/10

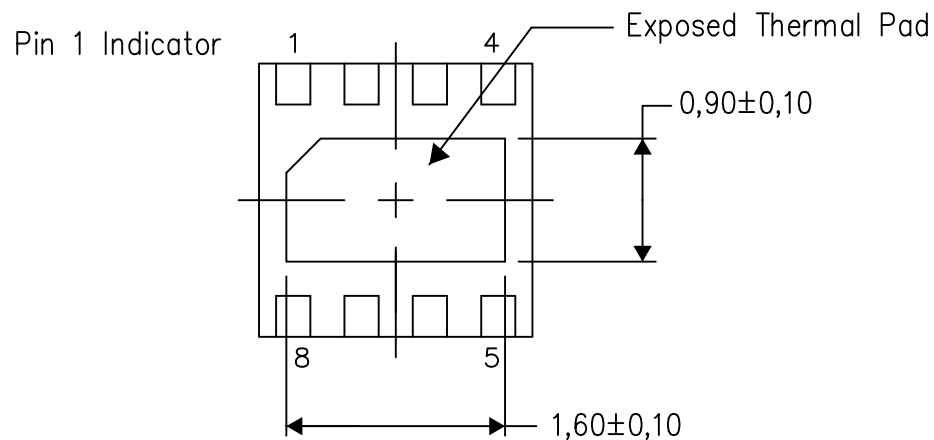
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-229.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

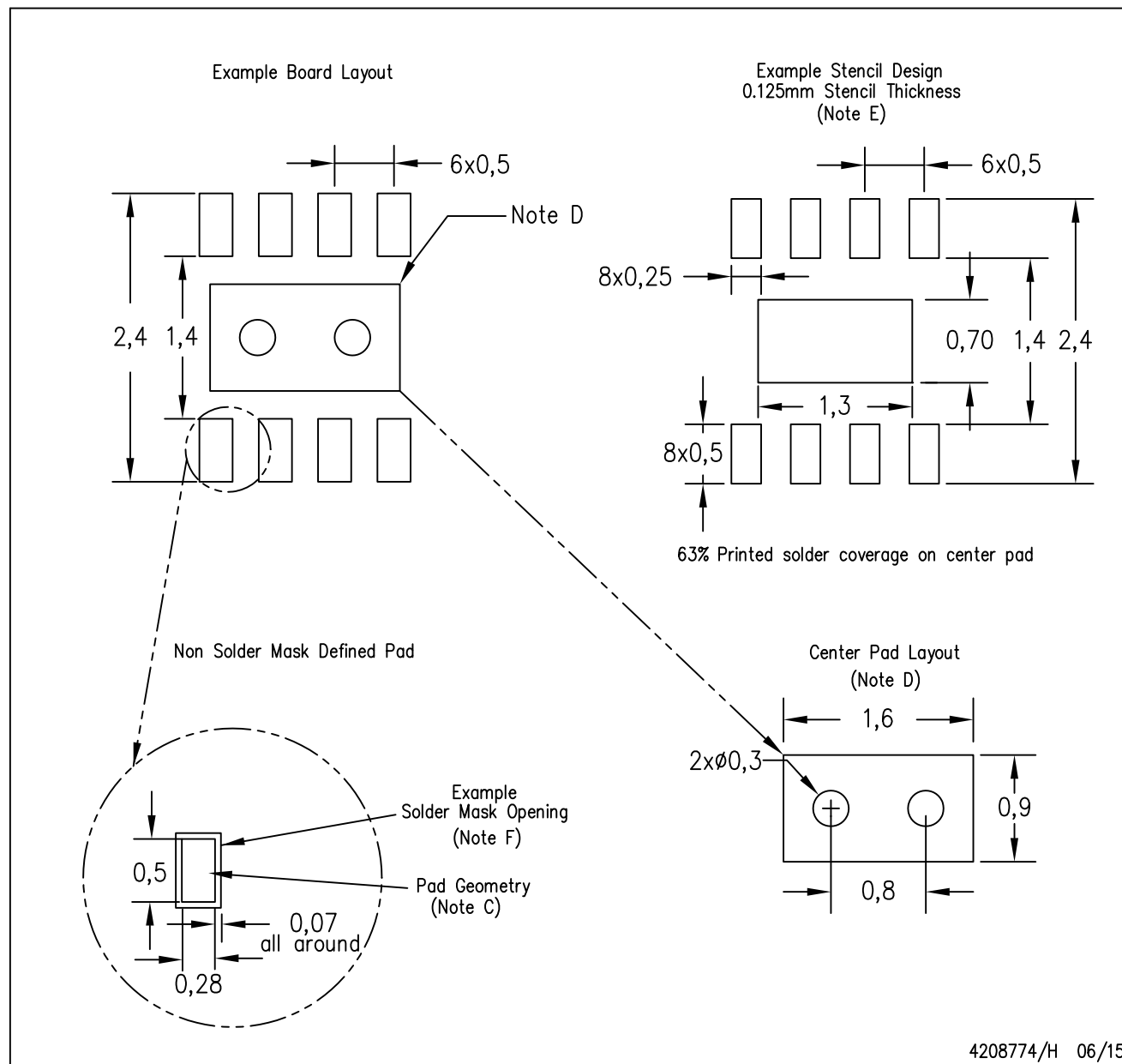
Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.