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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR **2SJ649**

# **SWITCHING** P-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The 2SJ649 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE
2SJ649	Isolated TO-220

#### **FEATURES**

· Low on-state resistance:

 $R_{DS(on)1} = 48 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -10 \text{ V}, I_D = -10 \text{ A)}$ 

 $R_{DS(on)2} = 75 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.0 \text{ V, Ip} = -10 \text{ A)}$ 

• Low input capacitance:

 $C_{iss} = 1900 \text{ pF TYP.} (V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V})$ 

• Built-in gate protection diode

(Isolated TO-220)

# ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Ves = 0 V)	Voss	-60	V
Gate to Source Voltage (Vps = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓20	Α
Drain Current (pulse) Note1	$I_{D(pulse)} = \mp 70$		Α
Total Power Dissipation (Tc = 25°C)	PT	25	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current Note2	IAS	-20	Α
Single Avalanche Energy Note2	Eas	40	mJ



**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -30 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = -20  $\rightarrow$  0 V

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# **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

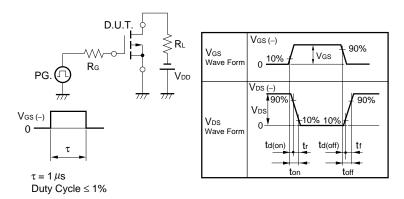
Characteristics	Symbol	Test Condtions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μΑ
Gate Leakage Current	Igss	V <sub>G</sub> S = ∓20 V, V <sub>D</sub> S = 0 V			∓10	μΑ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.5	-2.0	-2.5	V
Forward Transfer Admittance Note	yfs	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -10 A	10	20		S
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = -10 V, ID = -10 A		38	48	mΩ
	R <sub>DS(on)2</sub>	V <sub>G</sub> S = -4.0 V, I <sub>D</sub> = -10 A		47	75	mΩ
Input Capacitance	Ciss	Vps = −10 V		1900		pF
Output Capacitance	Coss	V <sub>G</sub> S = 0 V		350		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		140		pF
Turn-on Delay Time	td(on)	$V_{DD} = -30 \text{ V}, I_{D} = -10 \text{ A}$		10		ns
Rise Time	tr	V <sub>G</sub> S = -10 V		10		ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		73		ns
Fall Time	<b>t</b> f			17		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -48 V		38		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = -10 V		7		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -20 A		10		nC
Body Diode Forward Voltage Note	V <sub>F</sub> (S-D)	IF = 20 A, VGS = 0 V		0.95		V
Reverse Recovery Time	trr	IF = 20 A, VGS = 0 V		49		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		100		nC

**Note** Pulsed: PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

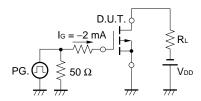
#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $V_{GS} = -20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$

#### **TEST CIRCUIT 2 SWITCHING TIME**

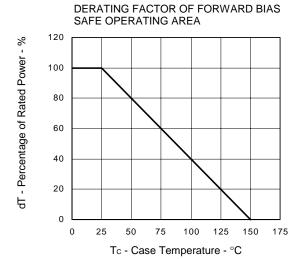


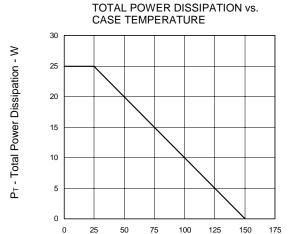
## **TEST CIRCUIT 3 GATE CHARGE**





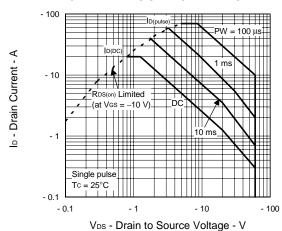
## TYPICAL CHARACTERISTICS (TA = 25°C)



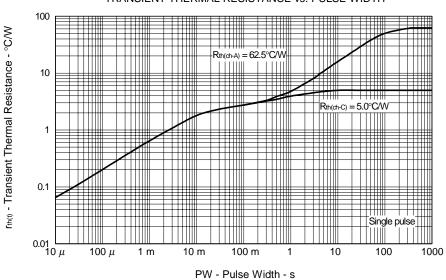


Tc - Case Temperature - °C

#### FORWARD BIAS SAFE OPERATING AREA



## TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

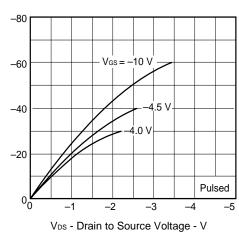


3

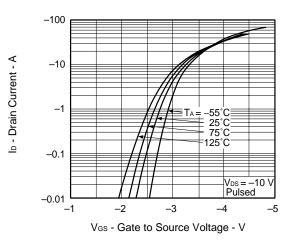
lo - Drain Current - A

Ves(off) - Gate Cut-off Voltage - V

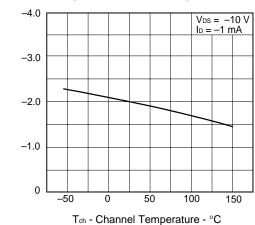
#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



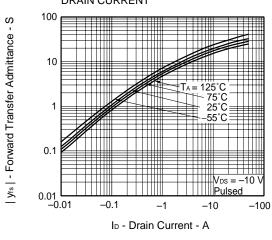
#### FORWARD TRANSFER CHARACTERISTICS



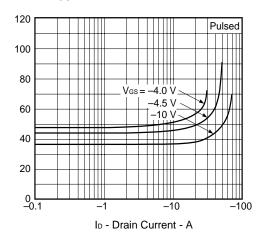
#### GATE CUT-OFF VOLTAGE vs. **CHANNEL TEMPERATURE**



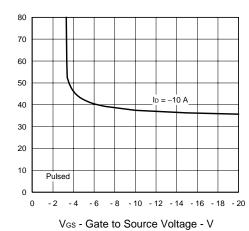
FORWARD TRANSFER ADMITTANCE vs. **DRAIN CURRENT** 



#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



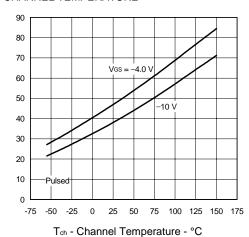
 $R_{DS(m)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

 $R_{DS(m)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

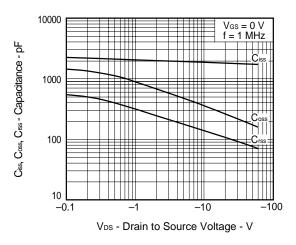
R<sub>DS(σ1)</sub> - Drain to Source On-state Resistance - mΩ

IF - Diode Forward Current - A

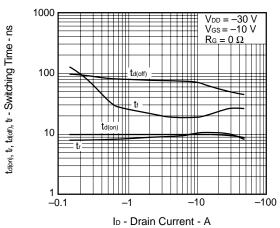
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



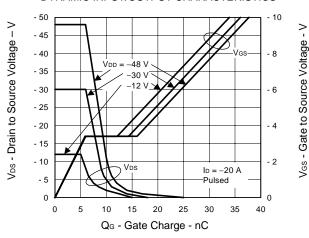
#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



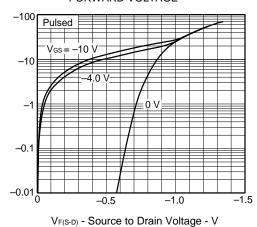
#### SWITCHING CHARACTERISTICS



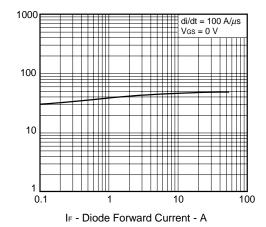
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



# SOURCE TO DRAIN DIODE FORWARD VOLTAGE



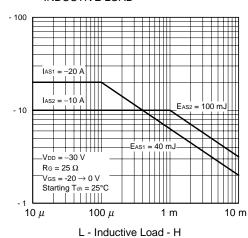
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



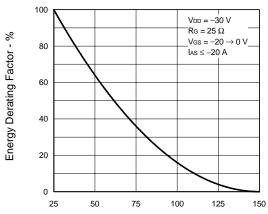
tr - Reverse Recovery Time - ns

IAS - Single Avalanche Current - A

# SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



# SINGLE AVALANCHE ENERGY DERATING FACTOR

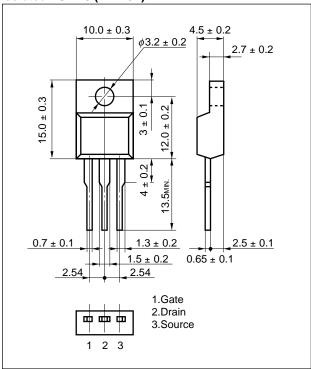


Starting T - Starting Channel Temperature -  $^{\circ}$ C

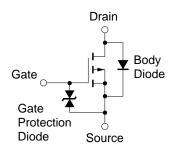


## PACKAGE DRAWING (Unit: mm)

# Isolated TO-220 (MP-45F)



## **EQUIVALENT CIRCUIT**



## Remark

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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