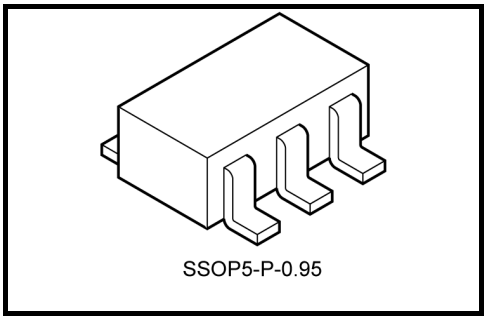
TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

# TAR5SB15 ~ TAR5SB50

Point Regulators (Low-Dropout Regulator)

The TAR5SBxx Series is comprised of general-purpose bipolar single-power-supply devices incorporating a control pin which can be used to turn them ON/OFF.

Overtemperature and overcurrent protection circuits are built in to the devices' output circuit.

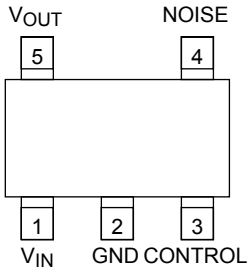



Weight: 0.014 g (typ.)

## Features

- Low stand-by current
- Overtemperature/overcurrent protection
- Operation voltage range is wide.
- Maximum output current is high.
- Difference between input voltage and output voltage is low.
- Small package. (SOT-23 5pin)
- Ceramic capacitors can be used.

## Pin Assignments (top view)




Overtemperature protection and overcurrent protection functions are not necessary guarantee of operating ratings below the absolute maximum ratings.

Do not use devices under conditions in which their absolute maximum ratings will be exceeded.

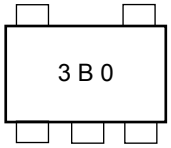
Start of commercial production
2002-09

## List of Products Number and Marking

| Products No. | Marking | Products No. | Marking |
|---|---|---|---|
| TAR5SB15 | 1B5 | TAR5SB33 | 3B3 |
| TAR5SB16 | 1B6 | TAR5SB34 | 3B4 |
| TAR5SB17 | 1B7 | TAR5SB35 | 3B5 |
| TAR5SB18 | 1B8 | TAR5SB36 | 3B6 |
| TAR5SB19 | 1B9 | TAR5SB37 | 3B7 |
| TAR5SB20 | 2B0 | TAR5SB38 | 3B8 |
| TAR5SB21 | 2B1 | TAR5SB39 | 3B9 |
| TAR5SB22 | 2B2 | TAR5SB40 | 4B0 |
| TAR5SB23 | 2B3 | TAR5SB41 | 4B1 |
| TAR5SB24 | 2B4 | TAR5SB42 | 4B2 |
| TAR5SB25 | 2B5 | TAR5SB43 | 4B3 |
| TAR5SB26 | 2B6 | TAR5SB44 | 4B4 |
| TAR5SB27 | 2B7 | TAR5SB45 | 4B5 |
| TAR5SB28 | 2B8 | TAR5SB46 | 4B6 |
| TAR5SB29 | 2B9 | TAR5SB47 | 4B7 |
| TAR5SB30 | 3B0 | TAR5SB48 | 4B8 |
| TAR5SB31 | 3B1 | TAR5SB49 | 4B9 |
| TAR5SB32 | 3B2 | TAR5SB50 | 5B0 |

## Marking on the Product

Example: TAR5SB30 (3.0 V output)




## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{IN}$ | 15 | V |
| Output current | $I_{OUT}$ | 200 | mA |
| Power dissipation | $P_D$ | 200 (Note 1) | mW |
| | | 380 (Note 2) | |
| Operation temperature range | $T_{opr}$ | −40 to 85 | °C |
| Storage temperature range | $T_{stg}$ | −55 to 150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Unit Ratintg

Note 2: Mounted on a glass epoxy circuit board of 30 × 30 mm. Pad dimension of 50 $mm^2$

## TAR5SB15~TAR5SB22

### Electrical Characteristic (unless otherwise specified, $V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 50$ mA, $C_{IN} = 1$ μF, $C_{OUT} = 10$ μF, $C_{NOISE} = 0.01$ μF, $T_j = 25°C$)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{OUT}$ | Please refer to the Output Voltage Accuracy table. | | | | |
| Line regulation | Reg·line | $V_{OUT} + 1$ V ≤ $V_{IN}$ ≤ 15 V, $I_{OUT} = 1$ mA | — | 3 | 15 | mV |
| Load regulation | Reg·load | 1 mA ≤ $I_{OUT}$ ≤ 150 mA | — | 25 | 75 | mV |
| Quiescent current | $I_{B1}$ | $I_{OUT} = 0$ mA | — | 170 | — | μA |
| | $I_{B2}$ | $I_{OUT} = 50$ mA | — | 550 | 850 | |
| Stand-by current | $I_{B\ (OFF)}$ | $V_{CT} = 0$ V | — | — | 0.1 | μA |
| Output noise voltage | $V_{NO}$ | $V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 10$ mA, 10 Hz ≤ f ≤ 100 kHz, $C_{NOISE} = 0.01$ μF, Ta = 25°C | — | 30 | — | $\mu V_{rms}$ |
| Temperature coefficient | $T_{CVO}$ | −40°C ≤ $T_{opr}$ ≤ 85°C | — | 100 | — | ppm/°C |
| Input voltage | $V_{IN}$ | — | 2.4 | — | 15 | V |
| Ripple rejection | R.R. | $V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 10$ mA, $C_{NOISE} = 0.01$ μF, f = 1 kHz, $V_{Ripple} = 500\ mV_{p-p}$, Ta = 25°C | — | 70 | — | dB |
| Control voltage (ON) | $V_{CT\ (ON)}$ | — | 1.5 | — | $V_{IN}$ | V |
| Control voltage (OFF) | $V_{CT\ (OFF)}$ | — | — | — | 0.4 | V |
| Control current (ON) | $I_{CT\ (ON)}$ | $V_{CT} = 1.5$ V | — | 3 | 10 | μA |
| Control current (OFF) | $I_{CT\ (OFF)}$ | $V_{CT} = 0$ V | — | 0 | 0.1 | μA |

## TAR5SB23~TAR5SB50

### Electrical Characteristic (unless otherwise specified, $V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 50$ mA, $C_{IN} = 1$ μF, $C_{OUT} = 10$ μF, $C_{NOISE} = 0.01$ μF, $T_j = 25°C$)

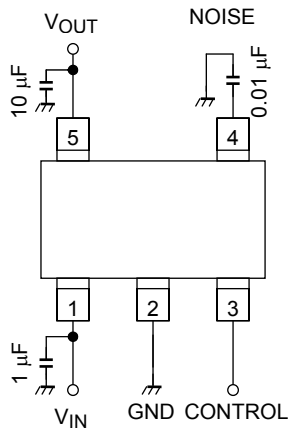
| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{OUT}$ | Please refer to the Output Voltage Accuracy table. | | | | |
| Line regulation | Reg·line | $V_{OUT} + 1$ V ≤ $V_{IN}$ ≤ 15 V, $I_{OUT} = 1$ mA | — | 3 | 15 | mV |
| Load regulation | Reg·load | 1 mA ≤ $I_{OUT}$ ≤ 150 mA | — | 25 | 75 | mV |
| Quiescent current | $I_{B1}$ | $I_{OUT} = 0$ mA | — | 170 | — | μA |
| | $I_{B2}$ | $I_{OUT} = 50$ mA | — | 550 | 850 | |
| Stand-by current | $I_{B\ (OFF)}$ | $V_{CT} = 0$ V | — | — | 0.1 | μA |
| Output noise voltage | $V_{NO}$ | $V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 10$ mA, 10 Hz ≤ f ≤ 100 kHz, $C_{NOISE} = 0.01$ μF, Ta = 25°C | — | 30 | — | $\mu V_{rms}$ |
| Dropout volatge | $V_{IN} - V_{OUT}$ | $I_{OUT} = 50$ mA | — | 130 | 200 | mV |
| Temperature coefficient | $T_{CVO}$ | −40°C ≤ $T_{opr}$ ≤ 85°C | — | 100 | — | ppm/°C |
| Input voltage | $V_{IN}$ | — | $V_{OUT}$ + 0.2 V | — | 15 | V |
| Ripple rejection | R.R. | $V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 10$ mA, $C_{NOISE} = 0.01$ μF, f = 1 kHz, $V_{Ripple} = 500\ mV_{p-p}$, Ta = 25°C | — | 70 | — | dB |
| Control voltage (ON) | $V_{CT\ (ON)}$ | — | 1.5 | — | $V_{IN}$ | V |
| Control voltage (OFF) | $V_{CT\ (OFF)}$ | — | — | — | 0.4 | V |
| Control current (ON) | $I_{CT\ (ON)}$ | $V_{CT} = 1.5$ V | — | 3 | 10 | μA |
| Control current (OFF) | $I_{CT\ (OFF)}$ | $V_{CT} = 0$ V | — | 0 | 0.1 | μA |

**Output Voltage Accuracy**
**($V_{IN}$ = $V_{OUT}$ + 1 V, $I_{OUT}$ = 50 mA, $C_{IN}$ = 1 μF, $C_{OUT}$ = 10 μF, $C_{NOISE}$ = 0.01 μF, $T_j$ = 25°C)**

| Product No. | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| TAR5SB15 | $V_{OUT}$ | 1.44 | 1.5 | 1.56 | V |
| TAR5SB16 | | 1.54 | 1.6 | 1.66 | |
| TAR5SB17 | | 1.64 | 1.7 | 1.76 | |
| TAR5SB18 | | 1.74 | 1.8 | 1.86 | |
| TAR5SB19 | | 1.84 | 1.9 | 1.96 | |
| TAR5SB20 | | 1.94 | 2.0 | 2.06 | |
| TAR5SB21 | | 2.04 | 2.1 | 2.16 | |
| TAR5SB22 | | 2.14 | 2.2 | 2.26 | |
| TAR5SB23 | | 2.24 | 2.3 | 2.36 | |
| TAR5SB24 | | 2.34 | 2.4 | 2.46 | |
| TAR5SB25 | | 2.43 | 2.5 | 2.57 | |
| TAR5SB26 | | 2.53 | 2.6 | 2.67 | |
| TAR5SB27 | | 2.63 | 2.7 | 2.77 | |
| TAR5SB28 | | 2.73 | 2.8 | 2.87 | |
| TAR5SB29 | | 2.83 | 2.9 | 2.97 | |
| TAR5SB30 | | 2.92 | 3.0 | 3.08 | |
| TAR5SB31 | | 3.02 | 3.1 | 3.18 | |
| TAR5SB32 | | 3.12 | 3.2 | 3.28 | |
| TAR5SB33 | | 3.21 | 3.3 | 3.39 | |
| TAR5SB34 | | 3.31 | 3.4 | 3.49 | |
| TAR5SB35 | | 3.41 | 3.5 | 3.59 | |
| TAR5SB36 | | 3.51 | 3.6 | 3.69 | |
| TAR5SB37 | | 3.6 | 3.7 | 3.8 | |
| TAR5SB38 | | 3.7 | 3.8 | 3.9 | |
| TAR5SB39 | | 3.8 | 3.9 | 4.0 | |
| TAR5SB40 | | 3.9 | 4.0 | 4.1 | |
| TAR5SB41 | | 3.99 | 4.1 | 4.21 | |
| TAR5SB42 | | 4.09 | 4.2 | 4.31 | |
| TAR5SB43 | | 4.19 | 4.3 | 4.41 | |
| TAR5SB44 | | 4.29 | 4.4 | 4.51 | |
| TAR5SB45 | | 4.38 | 4.5 | 4.62 | |
| TAR5SB46 | | 4.48 | 4.6 | 4.72 | |
| TAR5SB47 | | 4.58 | 4.7 | 4.82 | |
| TAR5SB48 | | 4.68 | 4.8 | 4.92 | |
| TAR5SB49 | | 4.77 | 4.9 | 5.03 | |
| TAR5SB50 | | 4.87 | 5.0 | 5.13 | |

## Application Note

### 1. Recommended Application Circuit




| Control Level | Operation |
|---|---|
| HIGH | ON |
| LOW | OFF |

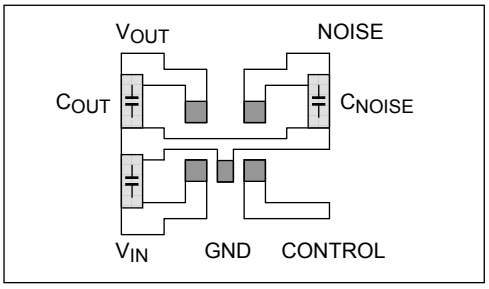
The figure above shows the recommended configuration for using a point regulator. Insert a capacitor for stable input/output operation.

If the control function is not to be used, Toshiba recommend that the control pin (pin 1) be connected to the $V_{CC}$ pin.

### 2. Power Dissipation

The power dissipation for board-mounted TAR5SBxx Series devices (rated at 380 mW) is measured using a board whose size and pattern are as shown below. When incorporating a device belonging to this series into your design, derate the power dissipation as far as possible by reducing the levels of parameters such as input voltage, output current and ambient temperature. Toshiba recommend that these devices should typically be derated to 70% to 80% of their absolute maximum power dissipation value.

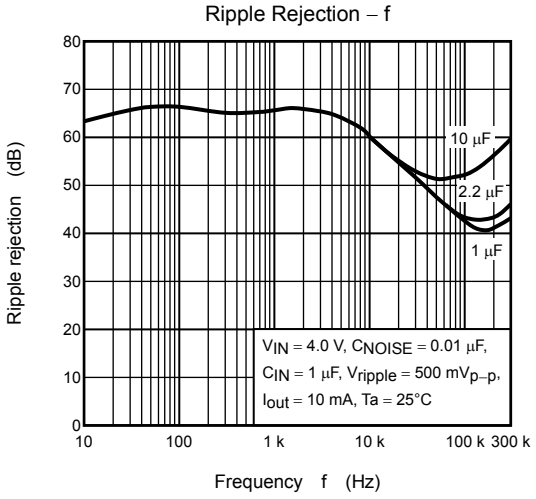
## Thermal Resistance Evaluation Board

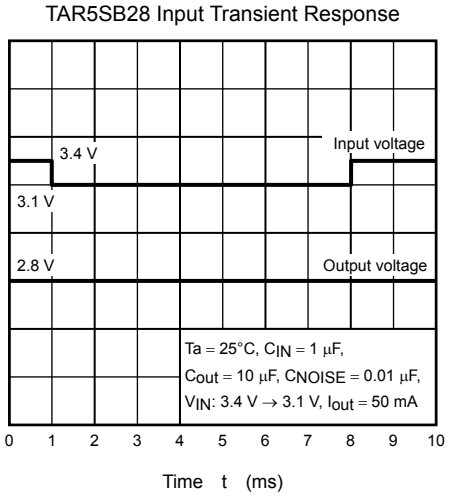



Circuit board material: glass epoxy,
Circuit board dimension: 30 mm × 30 mm,
Copper foil pad area: 50 $mm^2$ (t = 0.8 mm)

## 3. Ripple Rejection

The devices of the TAR5SBxx Series feature a circuit with an excellent ripple rejection characteristic. Because the circuit also features an excellent output fluctuation characteristic for sudden supply voltage drops, the circuit is ideal for use in the RF blocks incorporated in all mobile telephones.

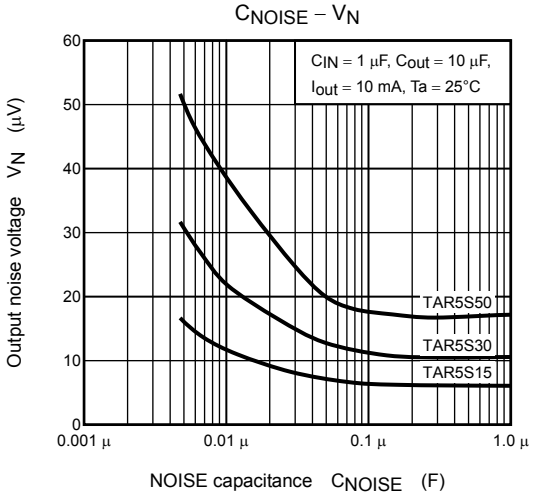


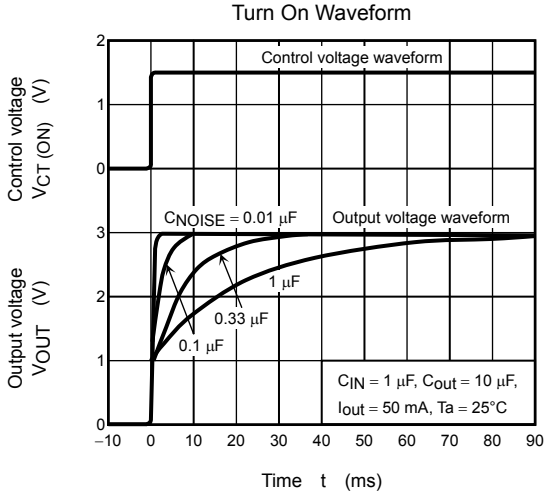




## 4. NOISE Pin

TAR5SBxx Series devices incorporate a NOISE pin to reduce output noise voltage. Inserting a capacitor between the NOISE pin and GND reduces output noise. To ensure stable operation, insert a capacitor of 0.0047 μF or more between the NOISE pin and GND.

The output voltage rise time varies according to the capacitance of the capacitor connected to the NOISE pin.



## 5. Example of Characteristics when Ceramic Capacitor is Used

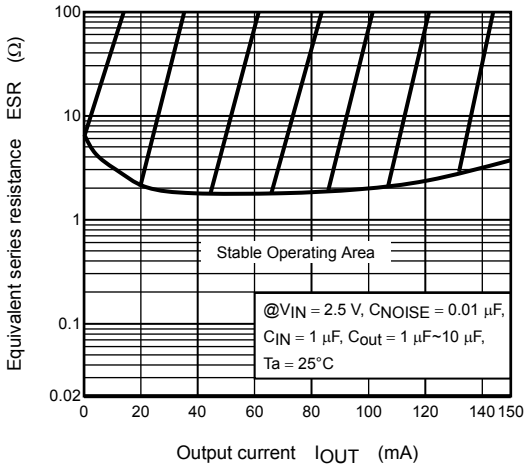
Shown below is the stable operation area, where the output voltage does not oscillate, evaluated using a Toshiba evaluation circuit. The equivalent series resistance (ESR) of the output capacitor and output current determines this area. TAR5SBxx Series devices operate stably even when a ceramic capacitor is used as the output capacitor.

If a ceramic capacitor is used as the output capacitor and the ripple frequency is 30 kHz or more, the ripple rejection differs from that when a tantalum capacitor is used. This is shown below.

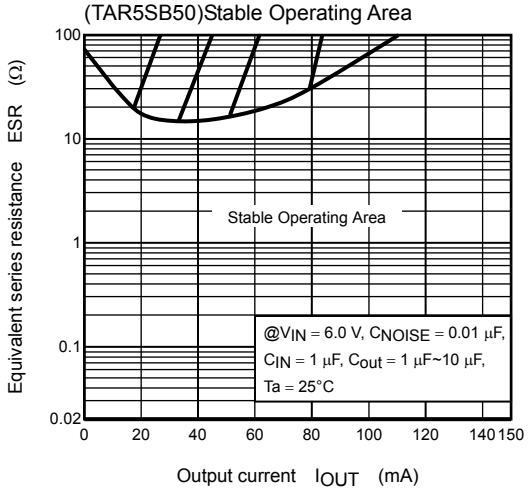
Toshiba recommend that users check that devices operate stably under the intended conditions of use.

### Examples of safe operating area characteristics

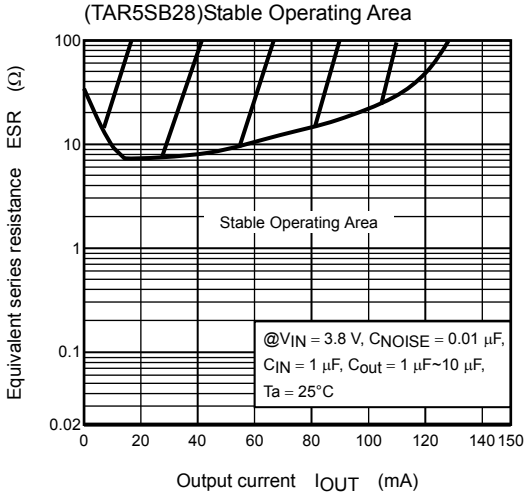
(TAR5SB15)Stable Operating Area



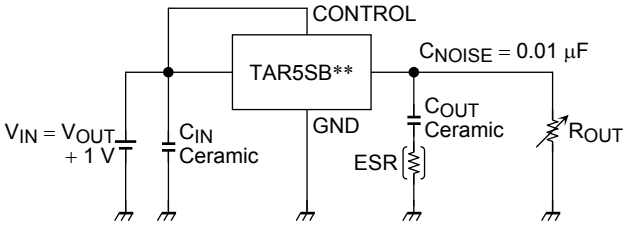

(TAR5SB50)Stable Operating Area




(TAR5SB28)Stable Operating Area



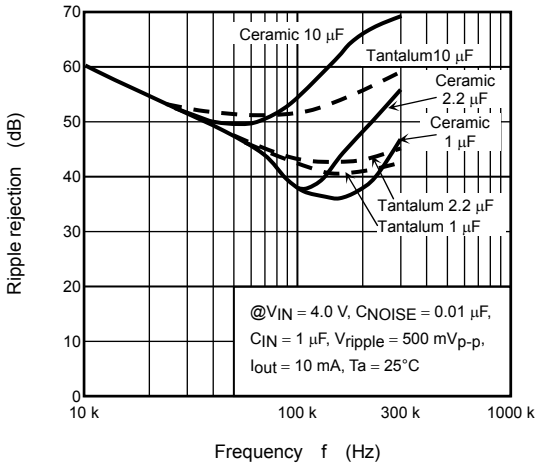

### Evaluation Circuit for Stable Operating Area



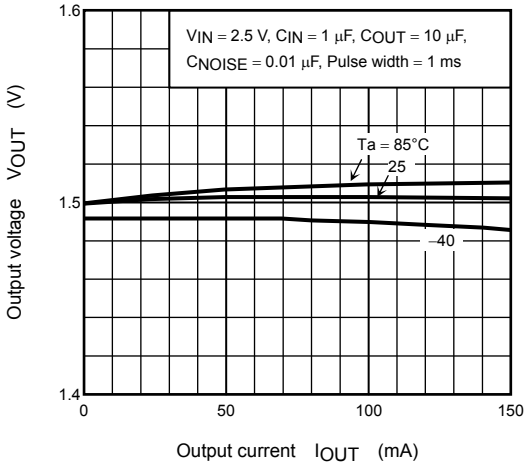

Capacitors used for evaluation
Made by Murata $C_{IN}$: GRM40B105K
$C_{OUT}$: GRM40B105K/GRM40B106K

### Ripple Rejection Characteristic (f = 10 kHz~300 kHz)

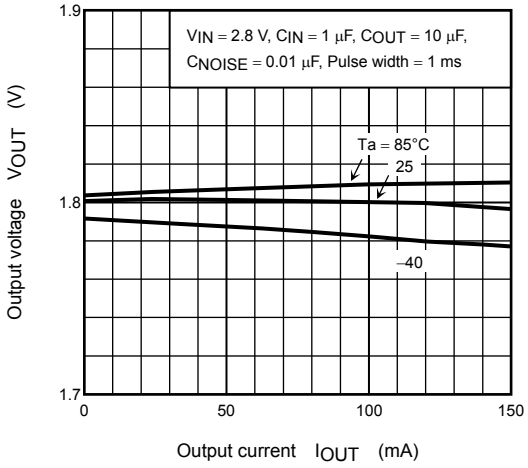
(TAR5SB30) Ripple Rejection – f



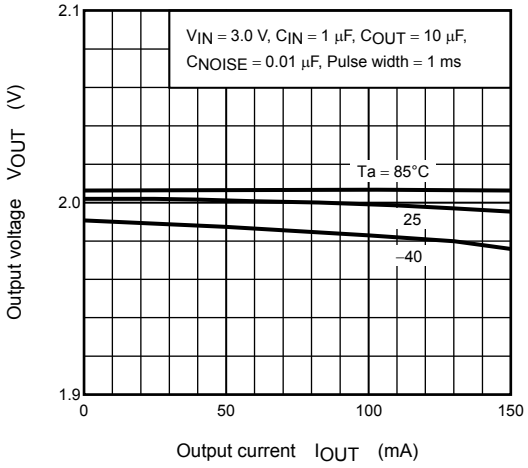
(TAR5SB15) $I_{OUT} - V_{OUT}$



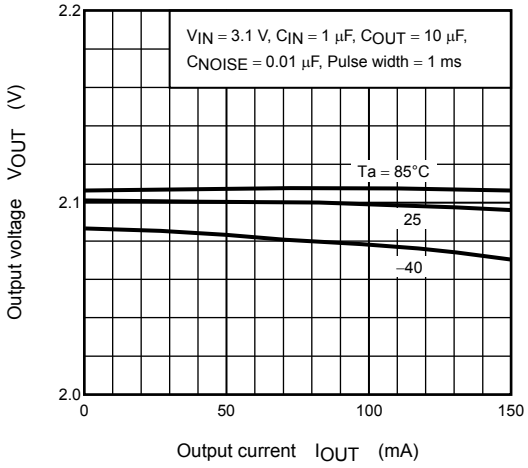

(TAR5SB18) $I_{OUT} - V_{OUT}$



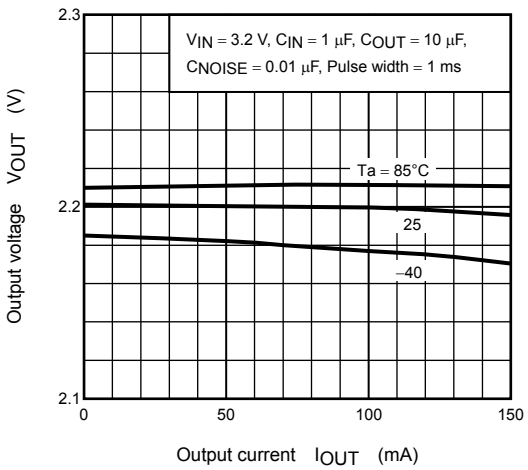

(TAR5SB20) $I_{OUT} - V_{OUT}$



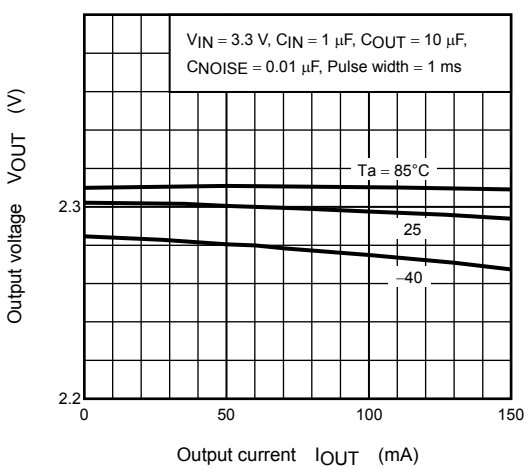

(TAR5SB21) $I_{OUT} - V_{OUT}$



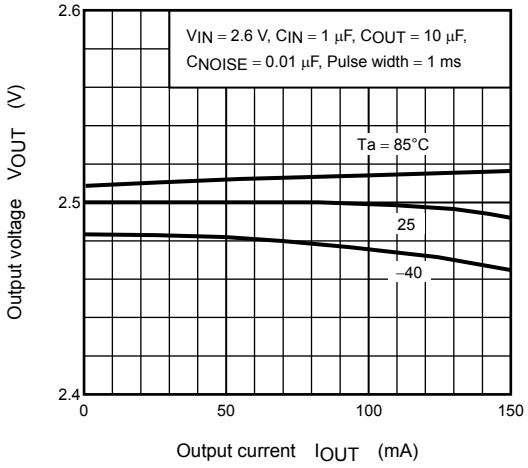

(TAR5SB22) $I_{OUT} - V_{OUT}$



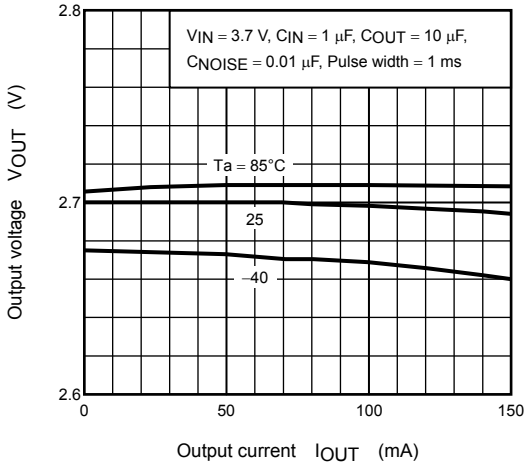

(TAR5SB23) $I_{OUT} - V_{OUT}$



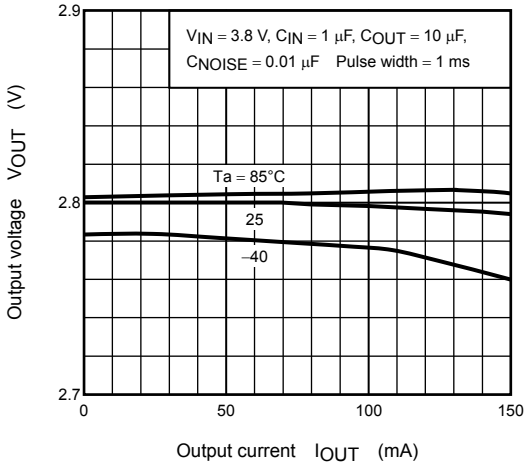
(TAR5SB25) $I_{OUT} - V_{OUT}$



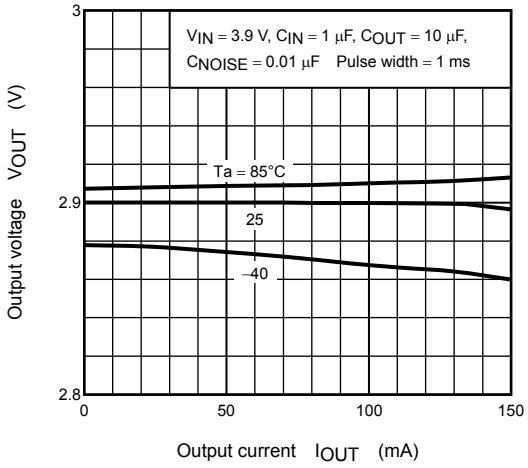

(TAR5SB27) $I_{OUT} - V_{OUT}$



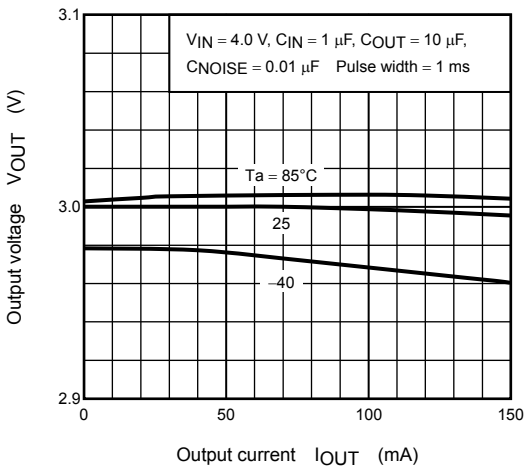

(TAR5SB28) $I_{OUT} - V_{OUT}$



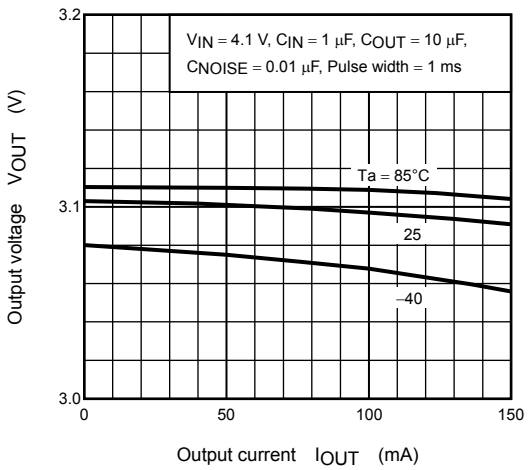

(TAR5SB29) $I_{OUT} - V_{OUT}$



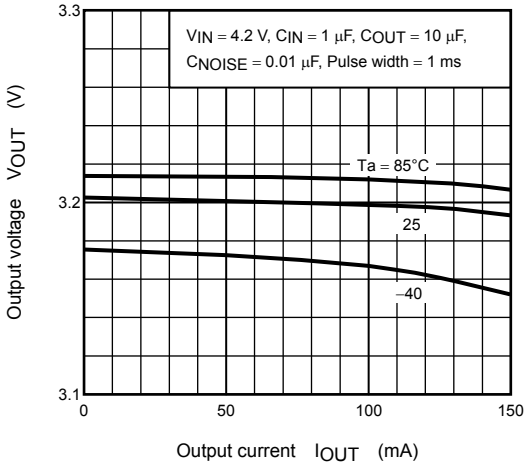

(TAR5SB30) $I_{OUT} - V_{OUT}$



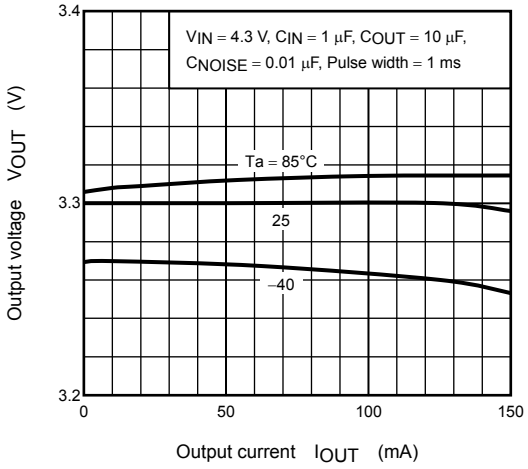

(TAR5SB31) $I_{OUT} - V_{OUT}$



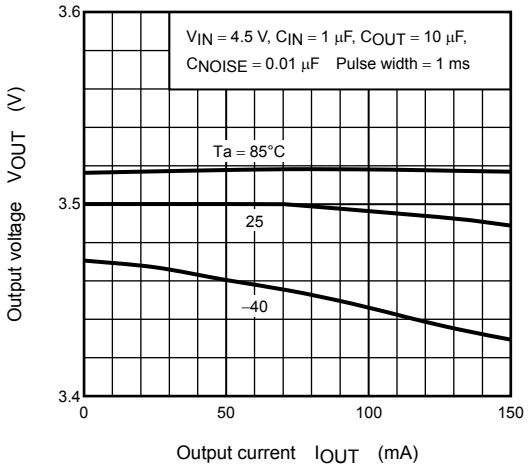
(TAR5SB32) $I_{OUT} - V_{OUT}$



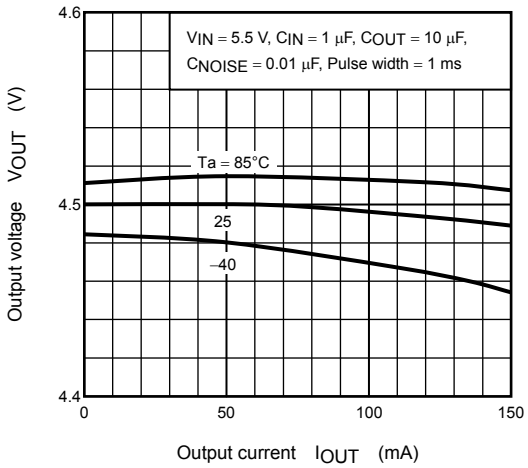

(TAR5SB33) $I_{OUT} - V_{OUT}$



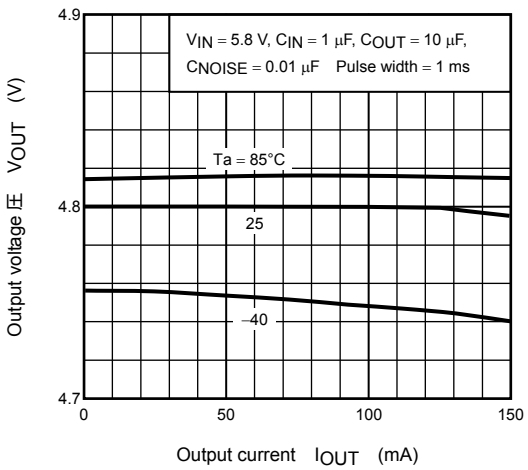

(TAR5SB35) $I_{OUT} - V_{OUT}$



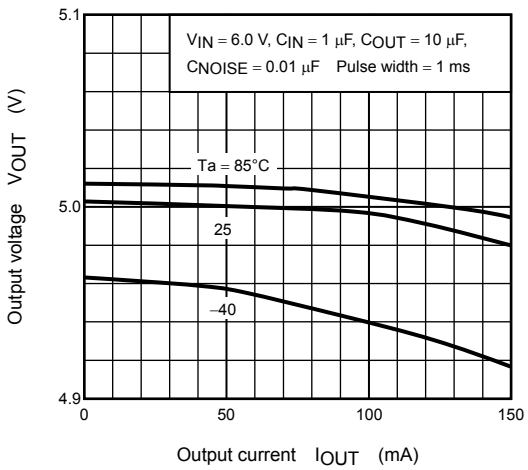

(TAR5SB45) $I_{OUT} - V_{OUT}$



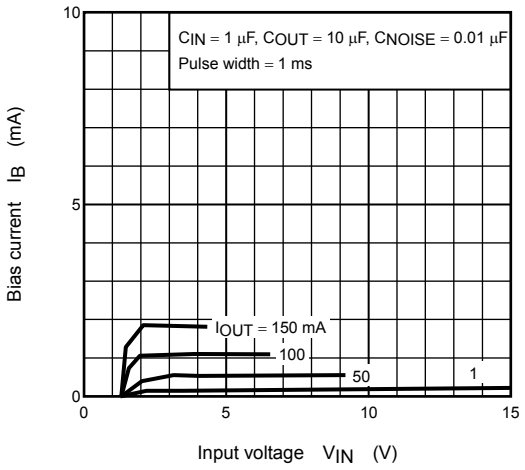

(TAR5SB48) $I_{OUT} - V_{OUT}$



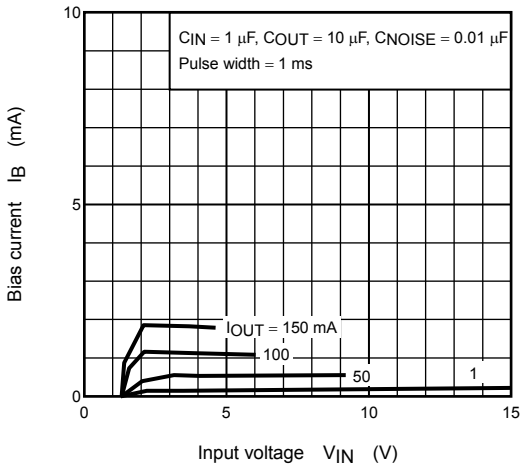

(TAR5SB50) $I_{OUT} - V_{OUT}$



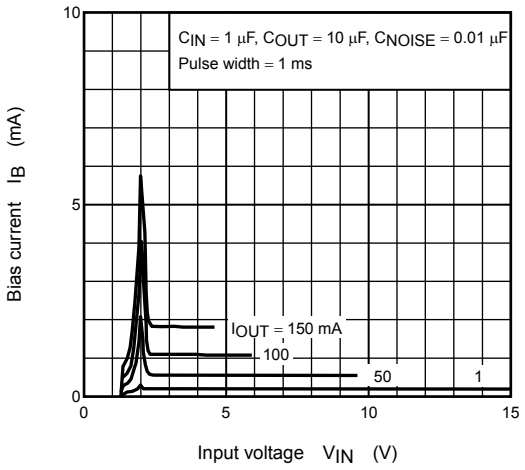
(TAR5SB15) $I_B - V_{IN}$



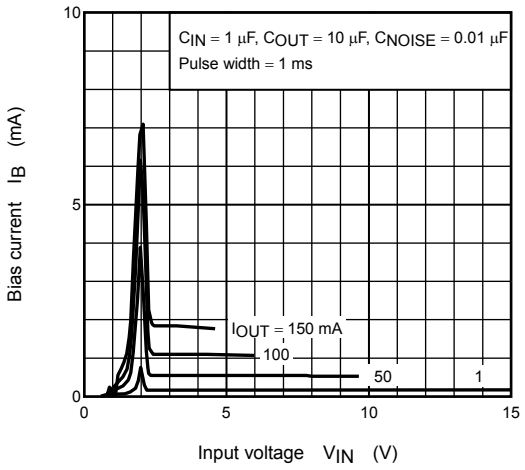

(TAR5SB18) $I_B - V_{IN}$



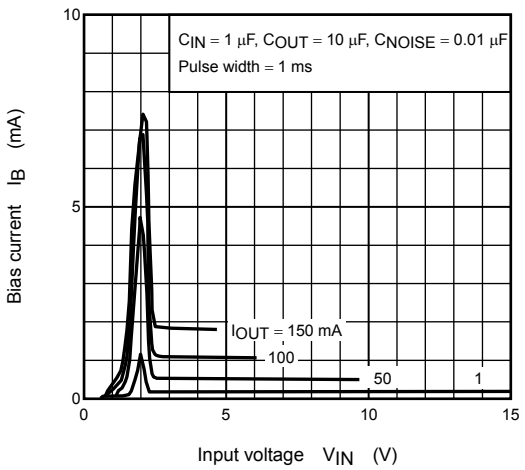

(TAR5SB20) $I_B - V_{IN}$



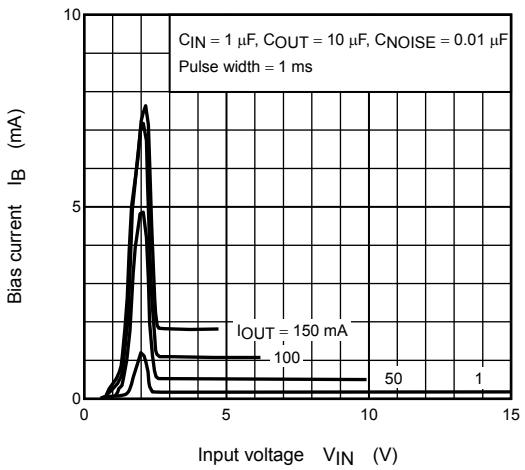

(TAR5SB21) $I_B - V_{IN}$



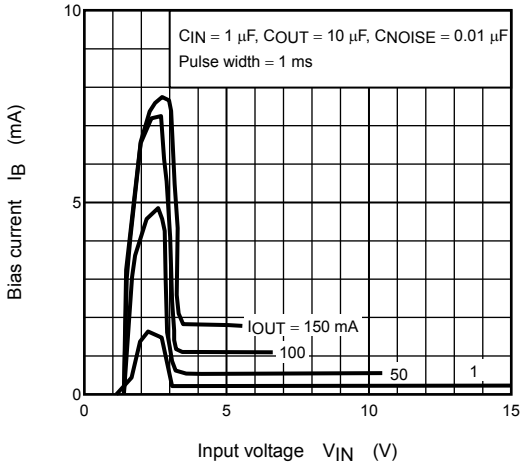

(TAR5SB22) $I_B - V_{IN}$



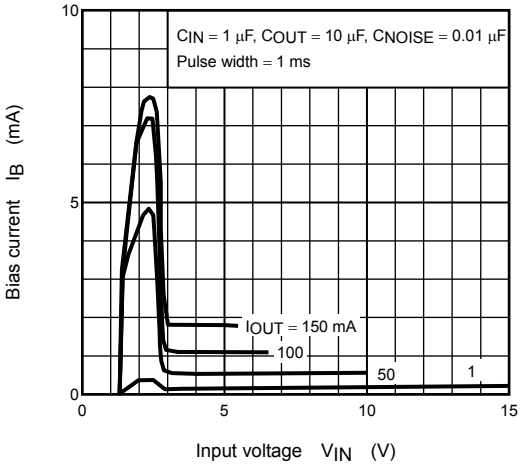

(TAR5SB23) $I_B - V_{IN}$



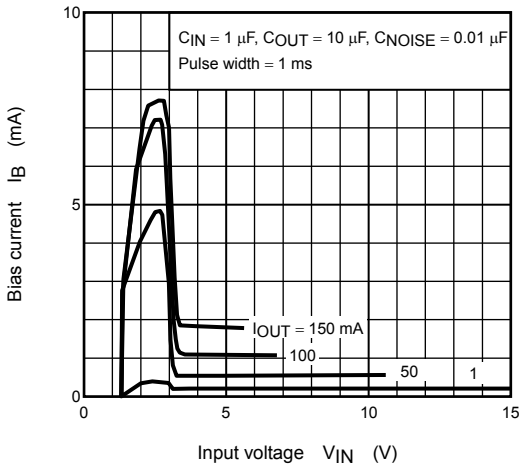
(TAR5SB25) $I_B - V_{IN}$



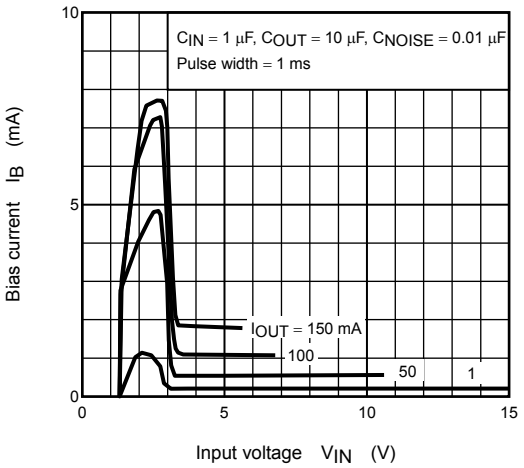

(TAR5SB27) $I_B - V_{IN}$



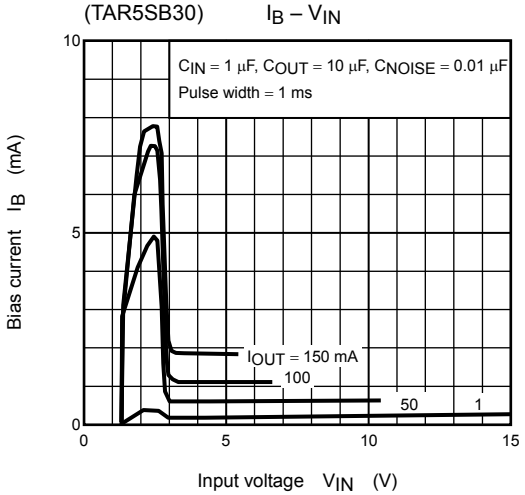

(TAR5SB28) $I_B - V_{IN}$



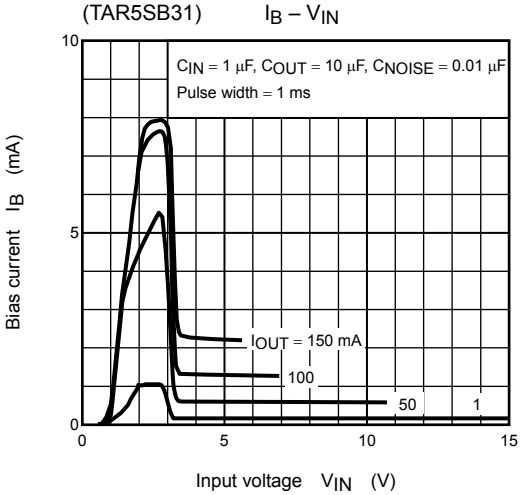

(TAR5SB29) $I_B - V_{IN}$



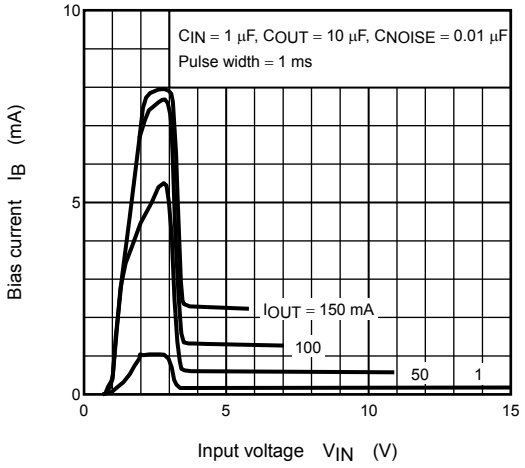

(TAR5SB30) $I_B - V_{IN}$



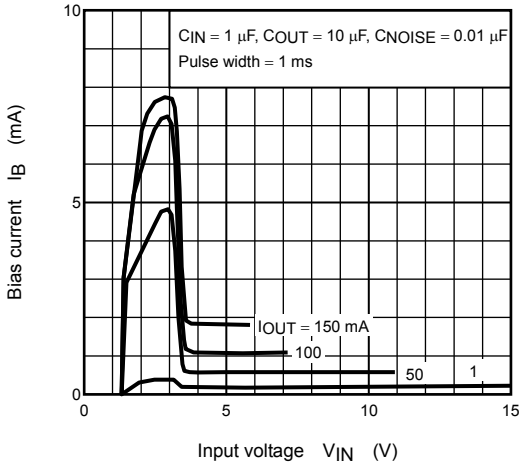

(TAR5SB31) $I_B - V_{IN}$



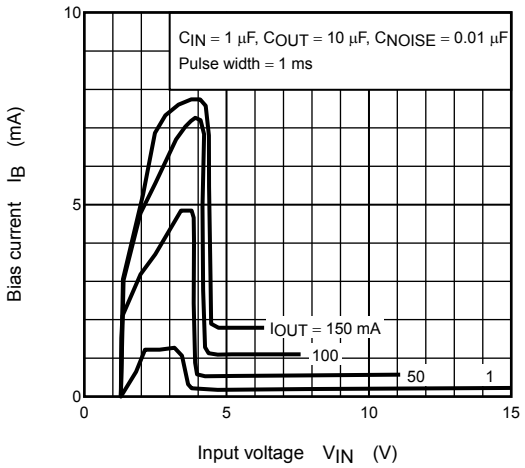
(TAR5SB32) $I_B - V_{IN}$



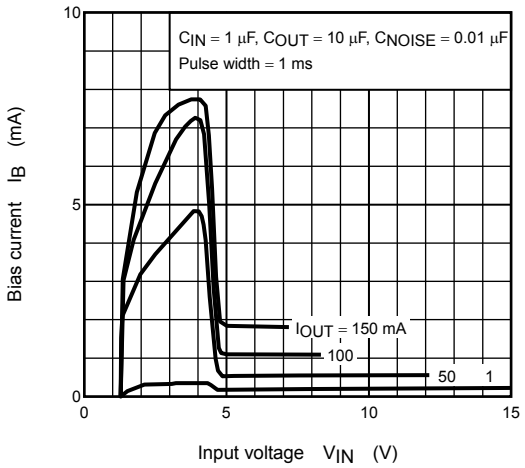

(TAR5SB33) $I_B - V_{IN}$



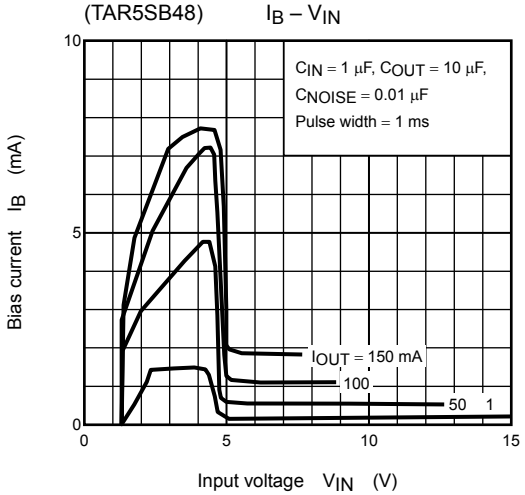

(TAR5SB35) $I_B - V_{IN}$



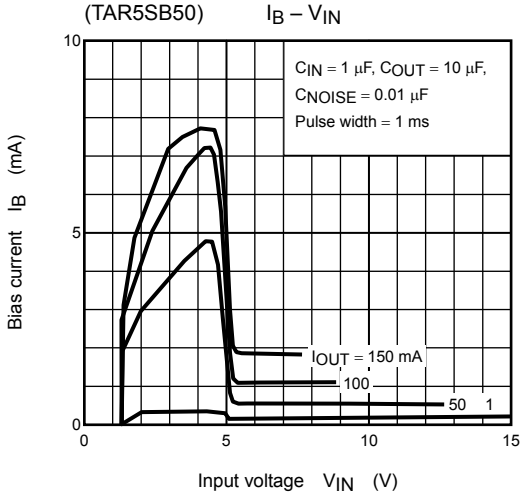

(TAR5SB45) $I_B - V_{IN}$



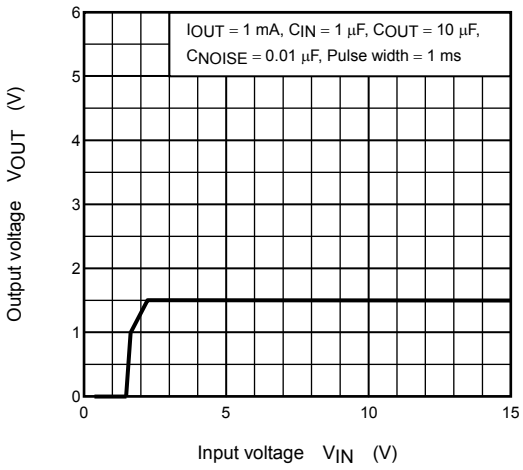

(TAR5SB48) $I_B - V_{IN}$



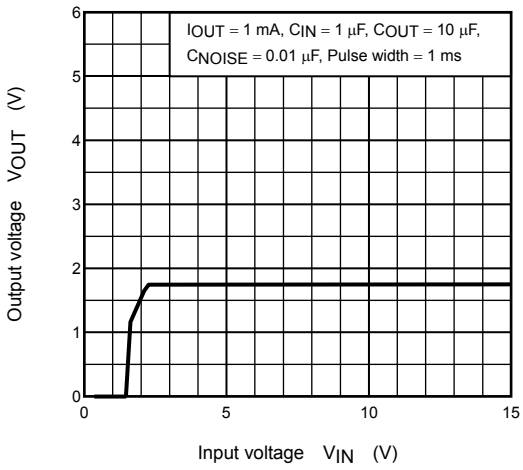

(TAR5SB50) $I_B - V_{IN}$



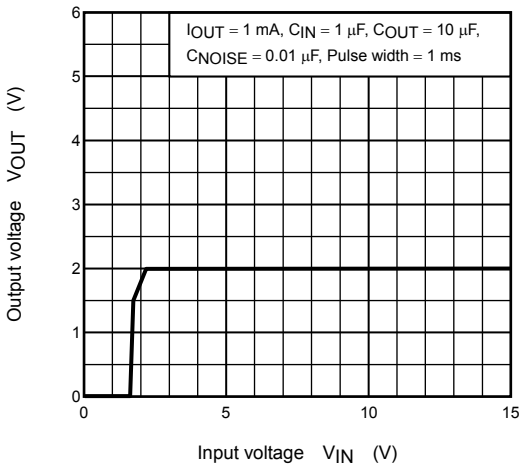
(TAR5SB15) $V_{OUT} - V_{IN}$



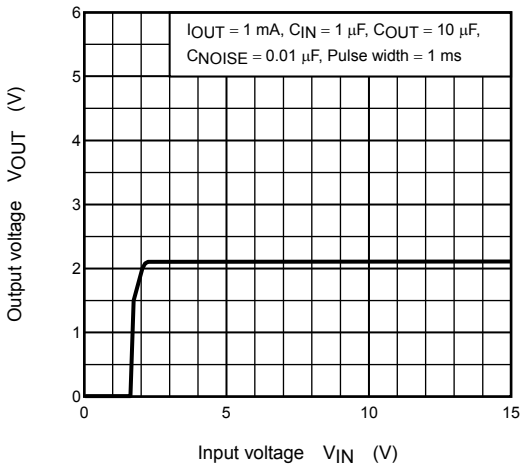

(TAR5SB18) $V_{OUT} - V_{IN}$



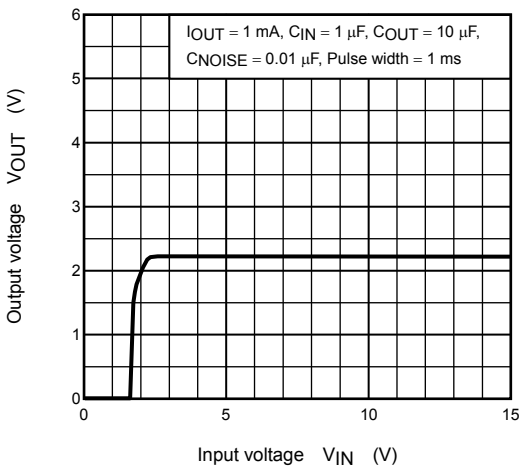

(TAR5SB20) $V_{OUT} - V_{IN}$



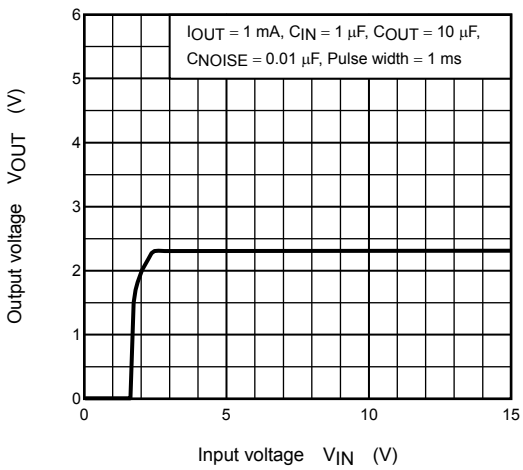

(TAR5SB21) $V_{OUT} - V_{IN}$



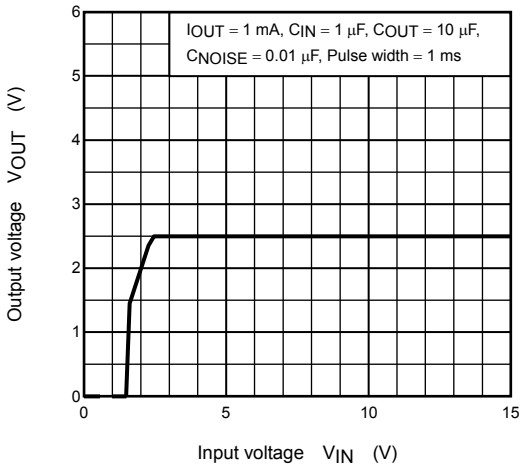

(TAR5SB22) $V_{OUT} - V_{IN}$



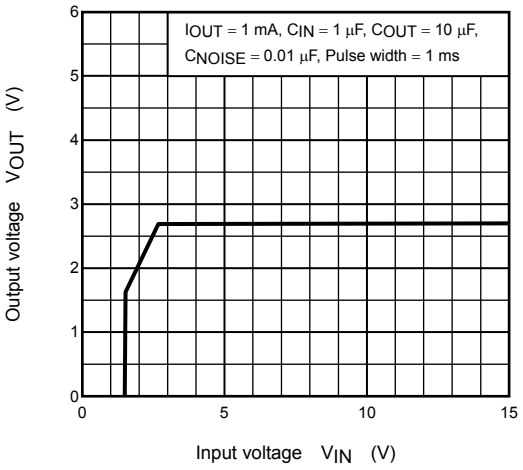

(TAR5SB23) $V_{OUT} - V_{IN}$



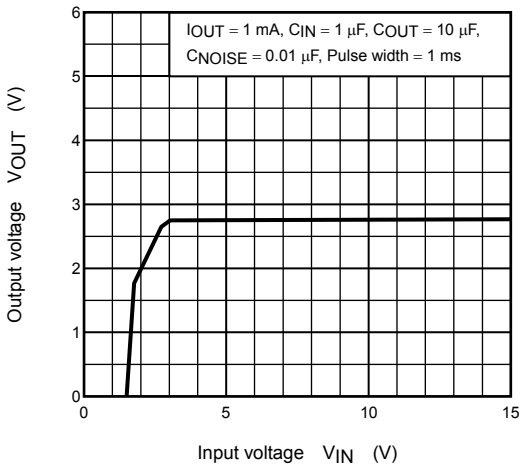
(TAR5SB25) $V_{OUT} - V_{IN}$



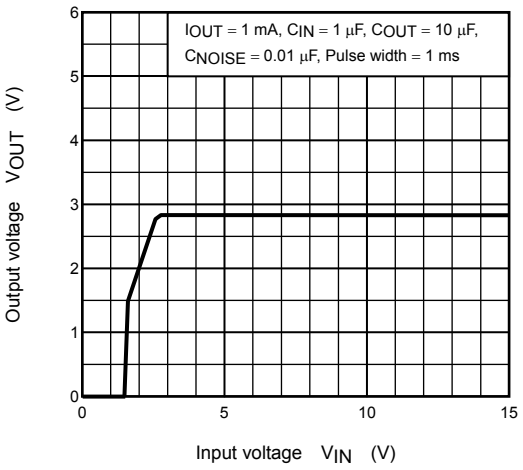

(TAR5SB27) $V_{OUT} - V_{IN}$



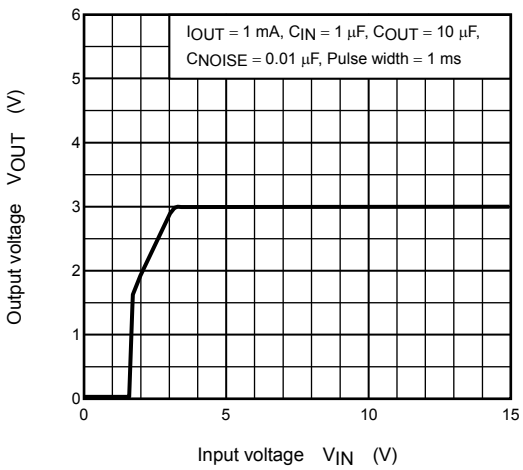

(TAR5SB28) $V_{OUT} - V_{IN}$



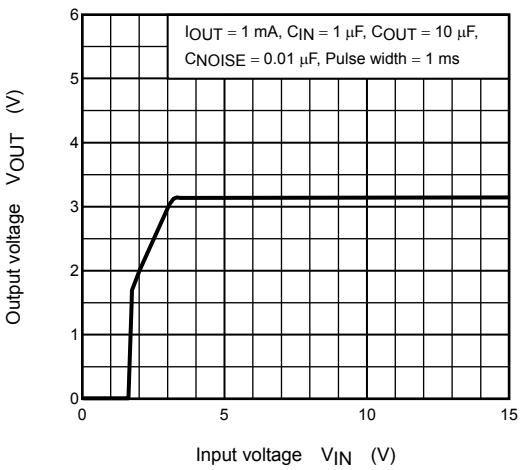

(TAR5SB29) $V_{OUT} - V_{IN}$



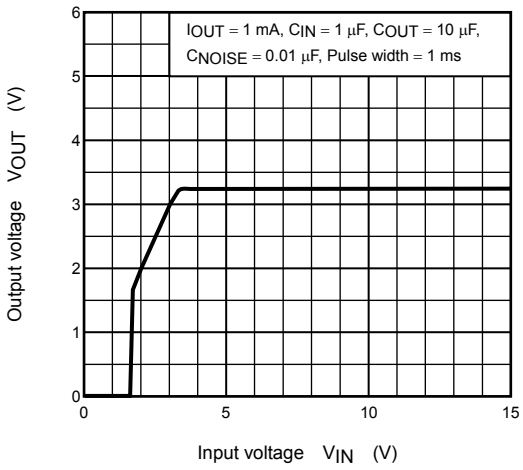

(TAR5SB30) $V_{OUT} - V_{IN}$



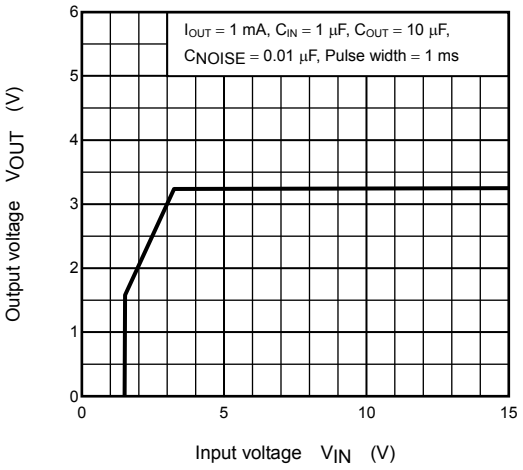

(TAR5SB31) $V_{OUT} - V_{IN}$



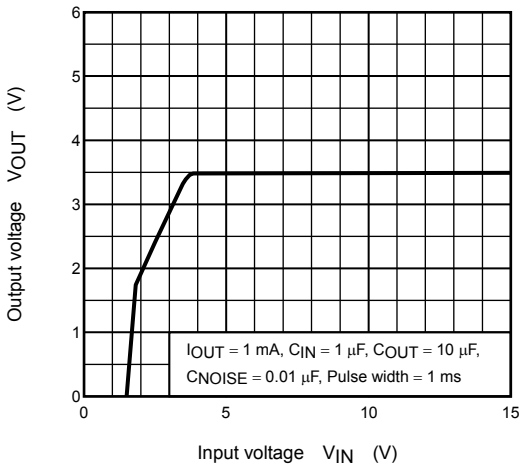
(TAR5SB32) $V_{OUT} - V_{IN}$



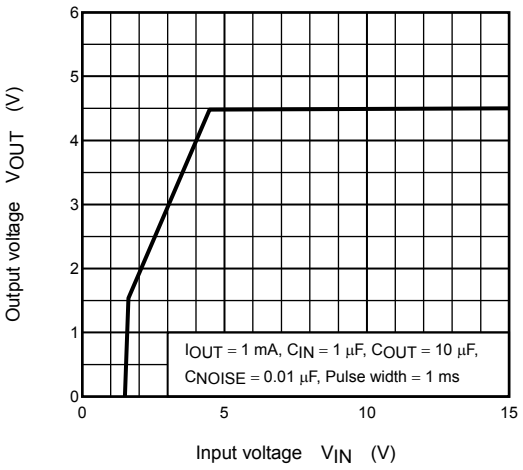

(TAR5SB33) $V_{OUT} - V_{IN}$



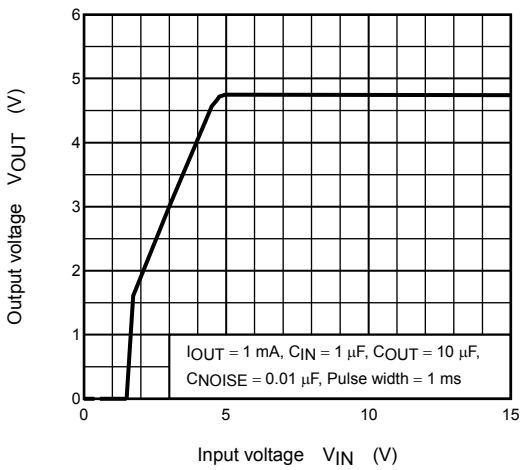

(TAR5SB35) $V_{OUT} - V_{IN}$



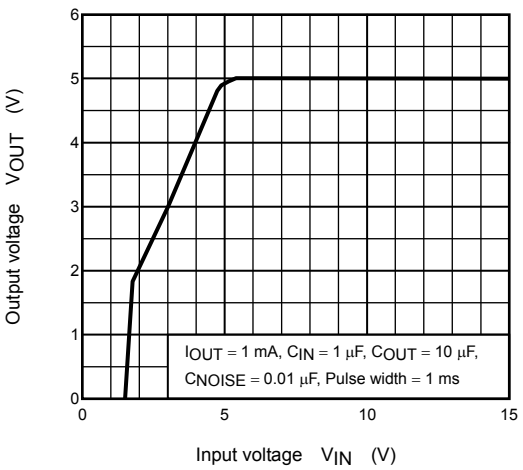

(TAR5SB45) $V_{OUT} - V_{IN}$



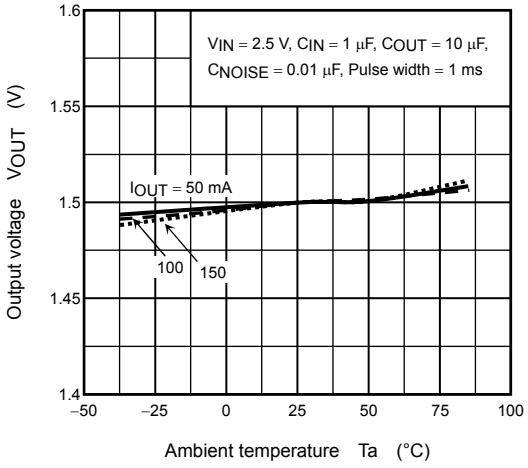

(TAR5SB48) $V_{OUT} - V_{IN}$



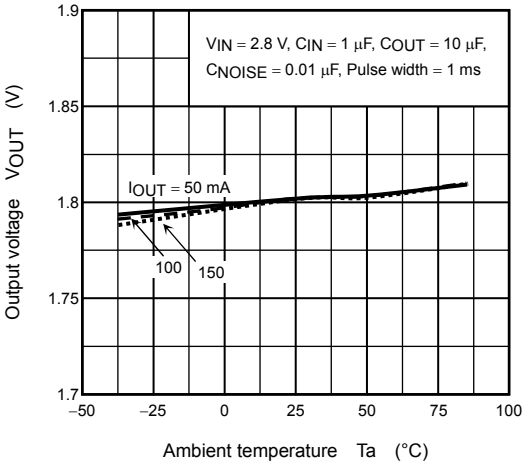

(TAR5SB50) $V_{OUT} - V_{IN}$



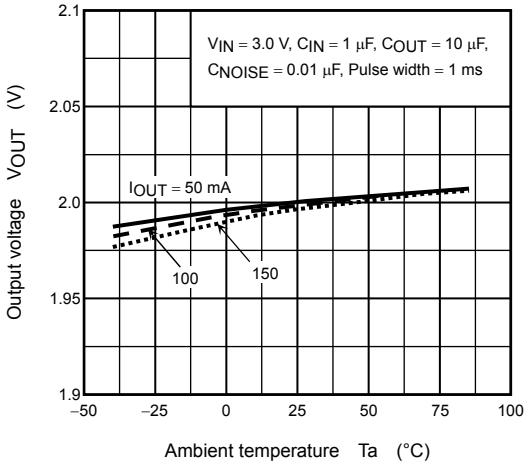
(TAR5SB15) $V_{OUT}$ – Ta



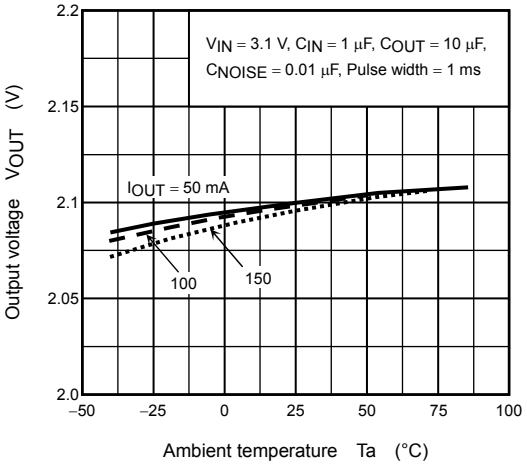

(TAR5SB18) $V_{OUT}$ – Ta



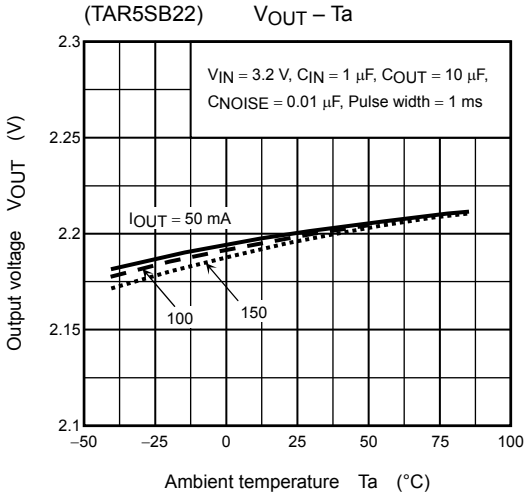

(TAR5SB20) $V_{OUT}$ – Ta



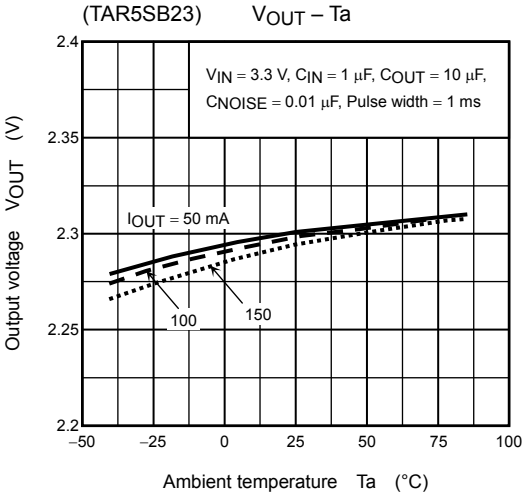

(TAR5SB21) $V_{OUT}$ – Ta



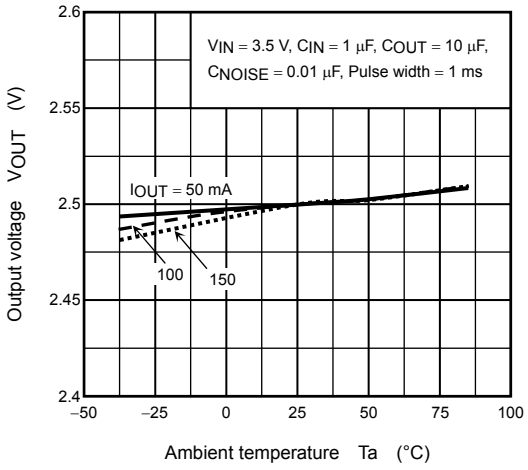

(TAR5SB22) $V_{OUT}$ – Ta



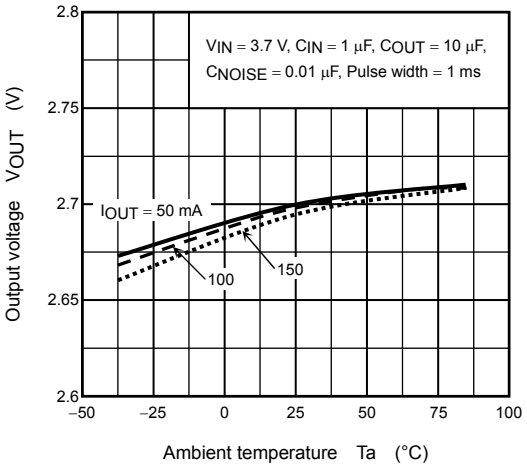

(TAR5SB23) $V_{OUT}$ – Ta



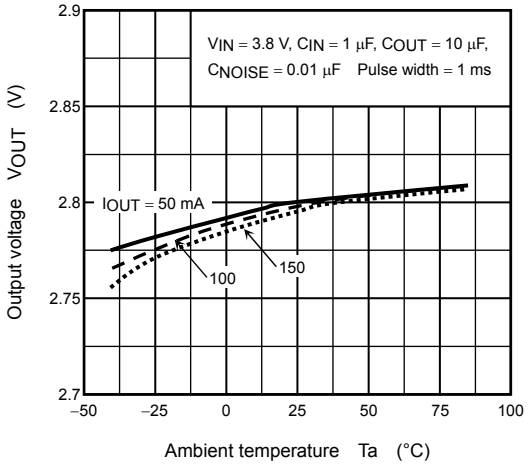
(TAR5SB25) $V_{OUT}$ – Ta



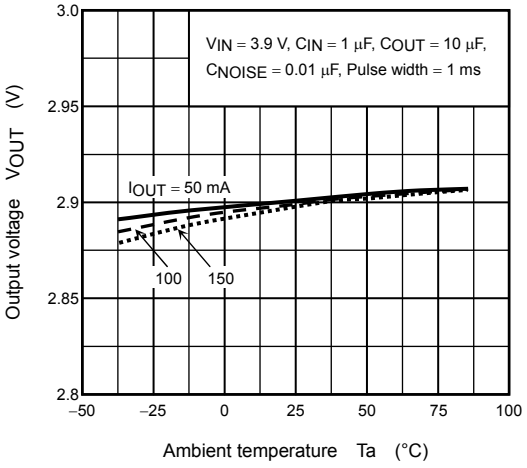

(TAR5SB27) $V_{OUT}$ – Ta



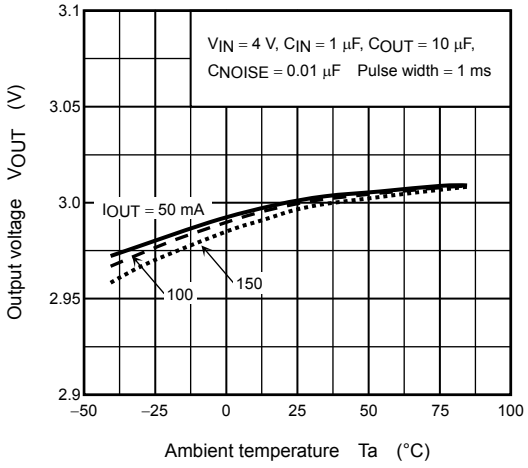

(TAR5SB28) $V_{OUT}$ – Ta



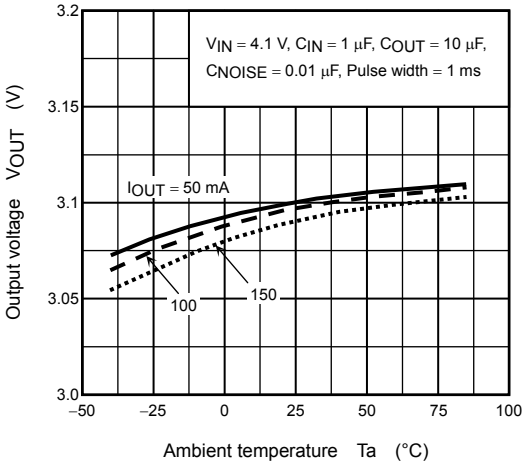

(TAR5SB29) $V_{OUT}$ – Ta



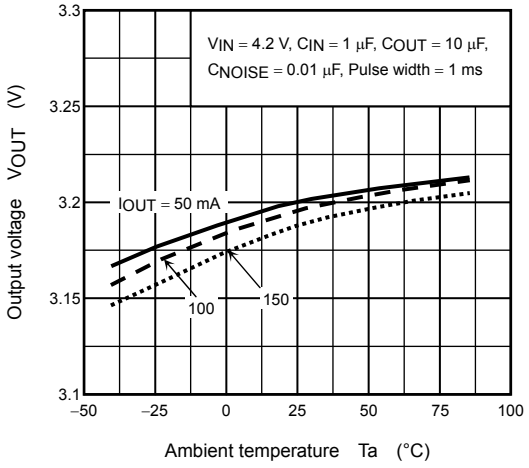

(TAR5SB30) $V_{OUT}$ – Ta



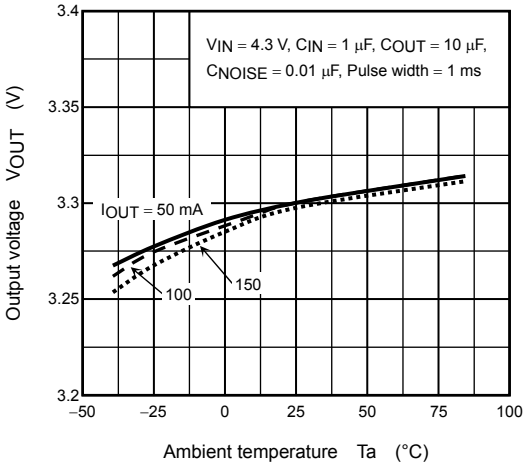

(TAR5SB31) $V_{OUT}$ – Ta



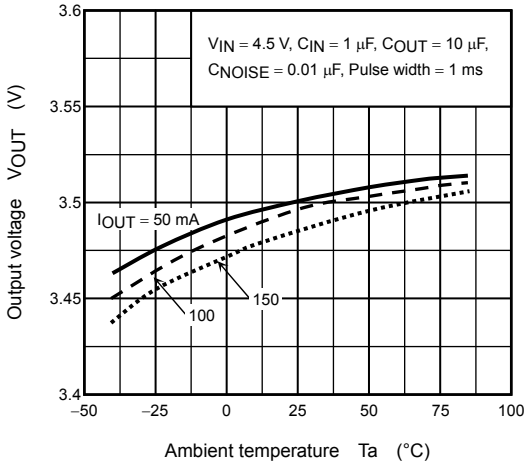
(TAR5SB32) $V_{OUT}$ – Ta



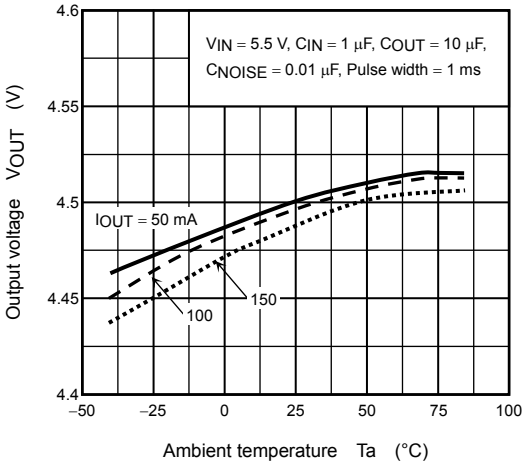

(TAR5SB33) $V_{OUT}$ – Ta



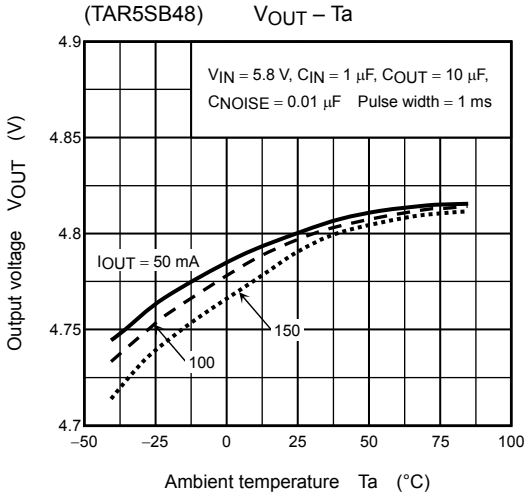

(TAR5SB35) $V_{OUT}$ – Ta



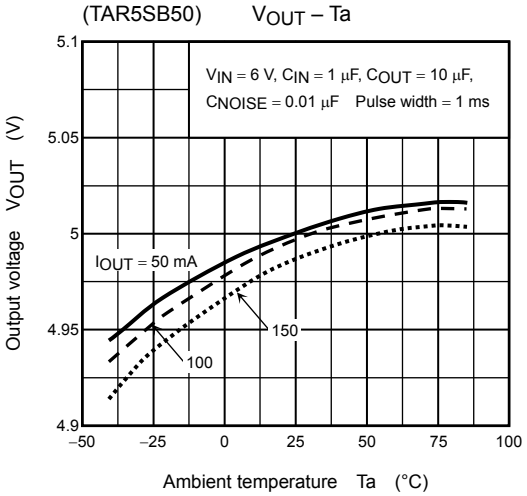

(TAR5SB45) $V_{OUT}$ – Ta



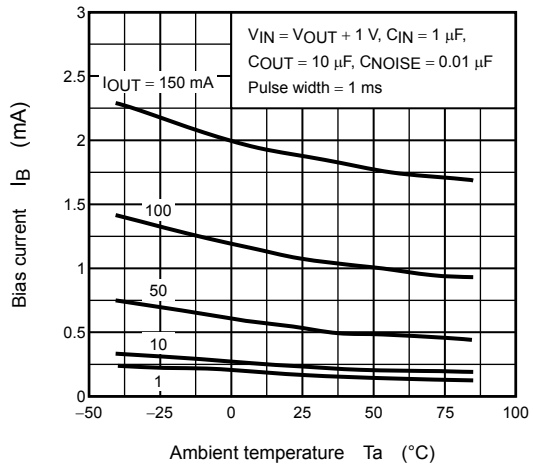

(TAR5SB48) $V_{OUT}$ – Ta



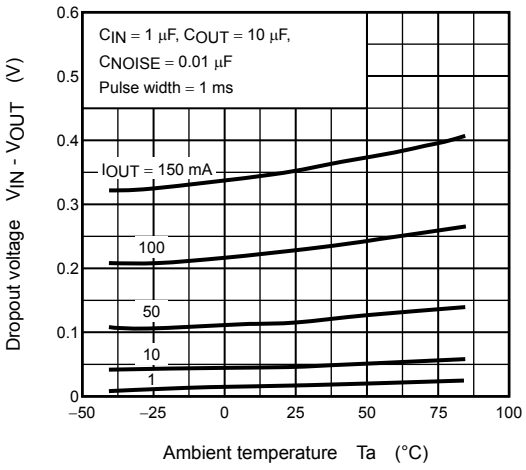

(TAR5SB50) $V_{OUT}$ – Ta



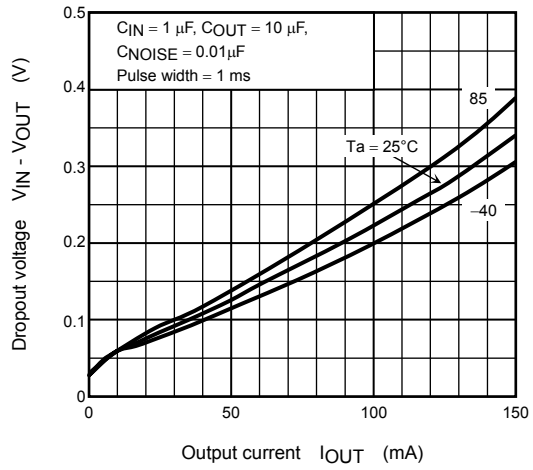
$I_B$ – Ta



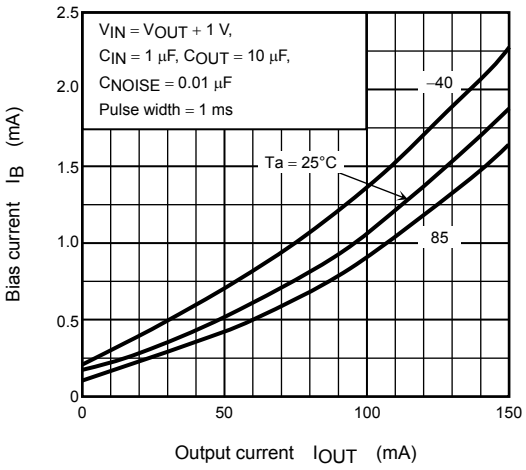

(TAR5SB23~TAR5SB50) $V_{IN}$ - $V_{OUT}$ – Ta



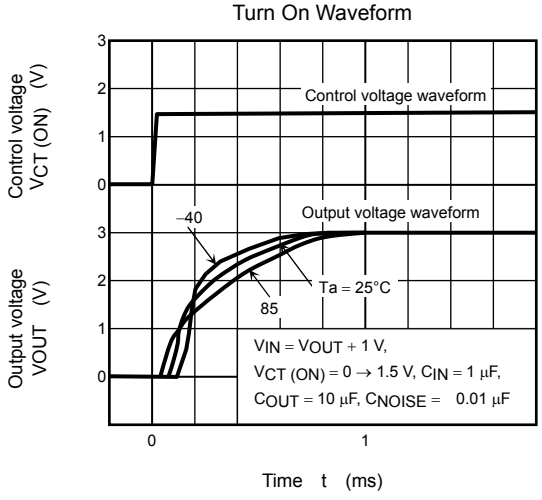

(TAR5SB23~TAR5SB50) $V_{IN}$ - $V_{OUT}$ – $I_{OUT}$



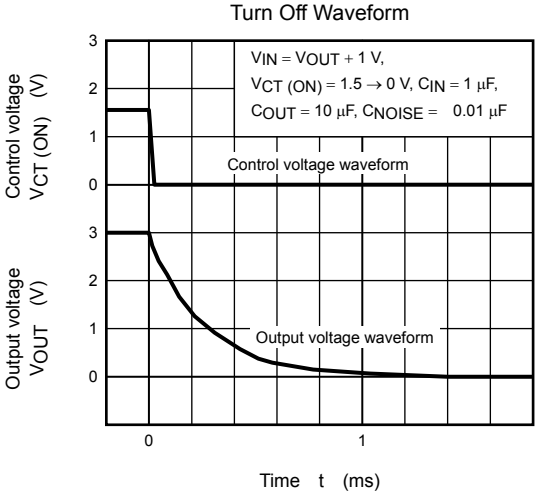

$I_B$ – $I_{OUT}$



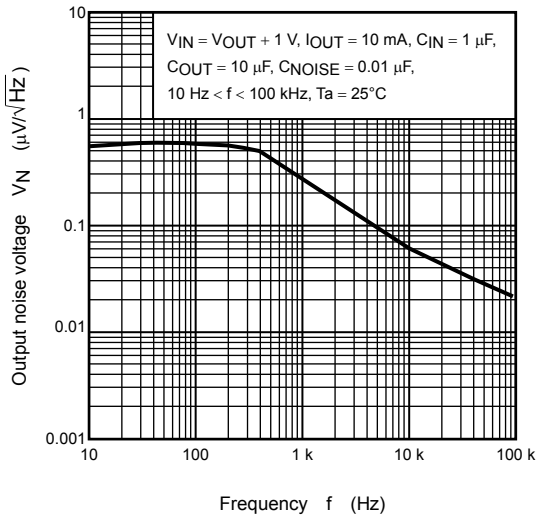

Turn On Waveform



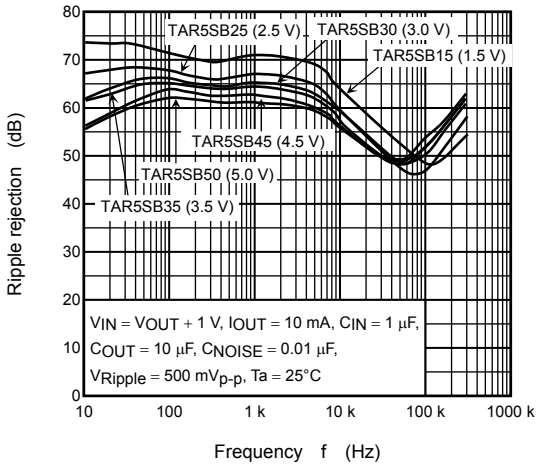

Turn Off Waveform



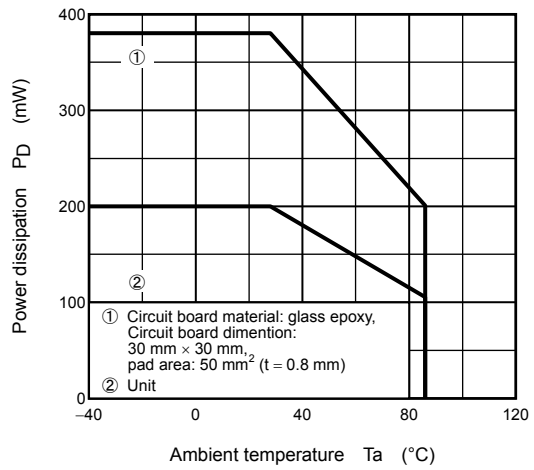
$V_N$ – f




Ripple Rejection – f

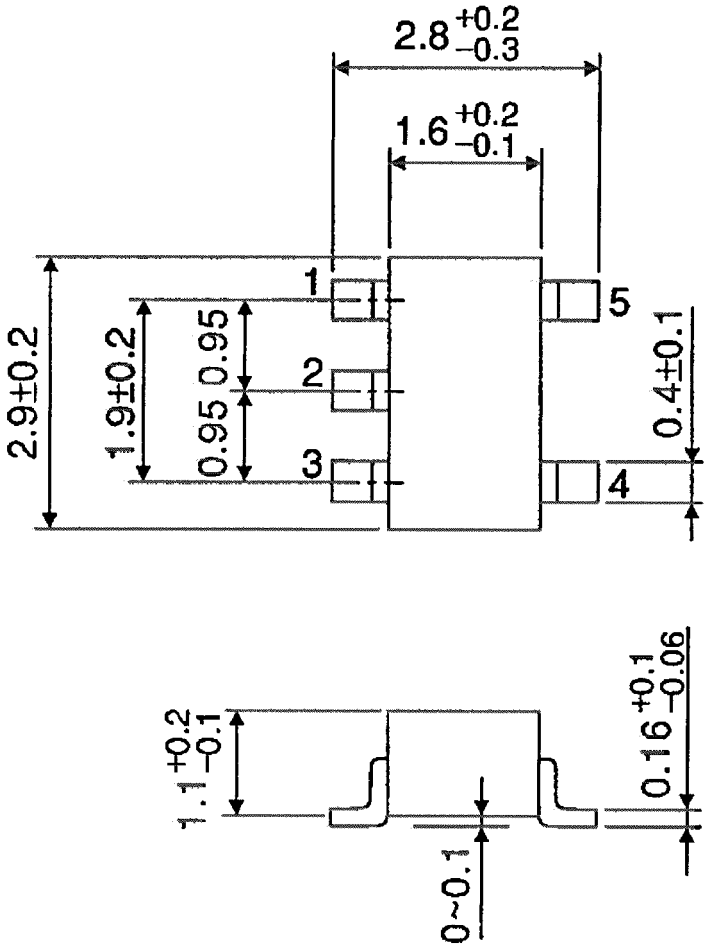



$P_D$ – Ta



**Package Dimensions**

SSOP5-P-0.95 Unit : mm




Weight: 0.014 g (typ.)

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